Stability Analysis of Series Connected SEPICs

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Abstract

The paper pioneers to introduce a feedback compensator network with a view to allow a stable operation of a series connected SEPIC system. It avails the role of a small signal model to predict its steady state stability and includes the use of compensators to ensure its stable operation. The ratio of its output to duty cycle transfer function characterizes its closed loop performance and suggests measures to bring the Eigen values of the characteristic equation to the left half of the S plane. The scheme incorporates the principle of average voltage sharing methodology to offer a stable servo and regulatory results over the range of operating loads. The strategy examined using MATLAB based Root locus and Bode plot analysis orchestrates its viability and utility in a practical environment.

Keywords:*series SEPIC, stability, compensator, average voltage sharing*

1. Introduction

Series connected dc-dc converters continue to find its use in high power applications that extend to aircraft power supplies and transit systems among others [1]. It provides an important advantage to regulate a larger power much more than its rated value at an overall efficiency greater than that of the original converter. The benefits include an ability to operate at relatively high dc bus voltages with reduced harmonic content, low EMI and low voltage stress on the devices [2].

The dc-dc converters in general adapt to the varying nature of the load and achieve high efficiency over a wide range of load currents. It is significant to keep the rate of change of the device voltage within safe limits to inflict a reliable operation during the switch transition. The operation espouses the need for a control technique to cope with their intrinsic nonlinearity and wide input voltage and load variations in order to elicit its stability in any operating condition.

The emergence of control techniques appear to address stability issues in series operation and evolve a breadth of solutions that facilitate to reach the loadability level. Among a plethora of strategies available in the literature, the use of compensators [3] resurfaces resurgence in this perspective and offers several advantages that embodies small-signal stability, robustness, good dynamic response and ease of implementation [4].

The stability analysis of a class of PWM dc-dc converter has been investigated through a systematic search of Lyapunov functions and there from the local region of attraction computed [5]. A modelling methodology based on average formulation has been developed for multiport dc-dc converters and provides scope to embed a control loop and arrive at complete small signal dynamic model [6].

A tractable mathematical stability analysis has been proposed to identify the fast scale instability of a voltage mode controlled dc-dc buck converter [7]. The performance of fully integrated dc-dc converter has been evaluated in terms of the converter loop stability analysis and its load transient response. The influence of the circuit inductor, output capacitor and feedback divider on the operation of the converter has been discussed [8].

An approach for series compensation of converters has been introduced to realize high efficiency and reduction in power rating of buck boost dc-dc converter [9]. The dynamic analysis of multiple connected power converter systems has been analyzed using nonlinear load sharing control technique realized through UC3907 [10].

However in view of the fact that converters connected in series augur to support high power applications, a new approach that be-hives uniform voltage sharing along with regulation of the output voltage and assuages steady state stability is significant in the prevailing environment.

2. Problem Formulation

The main focus revolves around the design of an appropriate feedback compensator that can be inserted in the small signal model of two SEPICs connected in series to extract its stable operation across the range of operating loads. The methodology envisages to establish its transfer function wherefrom the time and frequency domain stability is evaluated. The control algorithm extends to regulate the output voltage and equally share it between the two converters.

3. Proposed Strategy

The elaborate desire to attract the stable operation of power converters invites a rigorous analysis to ascertain its reliable operation. It enforces a renewed interest in control strategies for multiple connected converters that is in extensive use owing to growing consumer power demands, importance of dynamic power management, decrease of overall system cost, and growing requirements for system reliability and efficiency [11]. However, in spite of the seeming simplicity of dc-dc systems, the design of efficient control is intriguing in light of the nonlinearity, high dimensionality, and multi connectivity of the controlled system. The inherent difficulties associated with classical control design techniques resurge a nonlinear approach in the design format.

The power module seen in Fig. 1 includes two similar SEPICs energised using separate dc sources and connected in series at the output [12]. It serves to either step up or step down the input voltage of the same polarity and address the needs of high voltage applications.

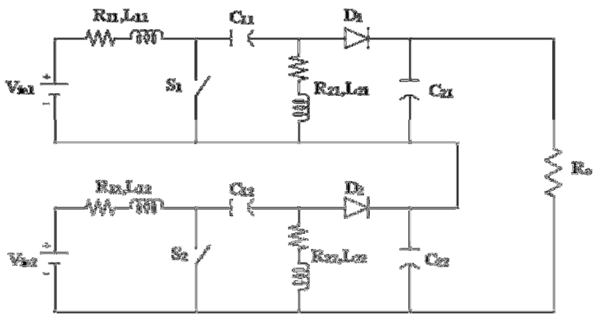

Fig. 1 Series connected SEPICs power module

4. Modeling

Modelling of a system may be described as a process of formulating a mathematical description of the system. It helps to establish a mathematical relationship among the input and output variables and thereby approximate the physical reality of a system [13]. The power converters which are truly nonlinear may be modelled either by sequential equations or a set of simultaneous equations in which at least one of them is required to be nonlinear [14]. The mathematical model enables an elaborate study of many small-signal phenomena using eigen value analysis and/or transfer functions.

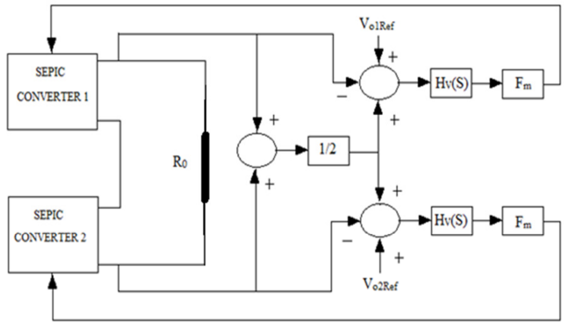

Fig.2 Series SEPICs with Average Voltage Control

The control algorithm explained through Fig.2 involves the philosophy of average sharing of voltage between the two converters connected in series at the output. It avails the role of a lead lag compensator which uses half of the desired output voltage as the reference to inflict uniform sharing of the voltage and regulate the load voltage. The compensator in other words is allowed to function as a closed loop controller and augurs the necessary change in the duty cycle in accordance with the mode of operation of the converter and the operating range of the converter. The theory reflects the entire action through width for the PWM pulses that in turn activate the power switches. It extends its theory to bring the eigen values of the composite characteristic equation formed as a product of the converter and compensator transfer functions to settle in the left half of the s- plane.

The transfer function model of a single SEPIC can be written as shown in equation (1)

$$\frac{V_0\ (S)}{d(S)} = \frac{1}{D^{'2}} \frac{\left(1-\frac{SL_1D^2}{RD^{'2}}\right)\left(1-\frac{SC_1\ (L_1+L_2)RD^{'2}}{L_1D^2}+\frac{S^2L_2C_1}{D}\right)}{\left(1+\frac{S}{\omega_{01}Q_1}+\frac{S^2}{\omega_{01}^2}\right)\left(1+\frac{S}{\omega_{02}Q_2}+\frac{S^2}{\omega_{02}^2}\right)} \quad (1)$$

Where

$$\omega_{01=} \frac{1}{\sqrt{L_1\left(C_2\frac{D^2}{D^{'2}}+C_1\right)+L_2(C_1+C_2)}} \quad (2)$$

$$Q_1 = \frac{R}{\omega_{01}\left(L_1\frac{D^2}{D^{'2}}+L_2\right)} \quad (3)$$

$$\omega_{02} = \sqrt{\frac{1}{L_2\frac{C_1}{D^2}\|\frac{C_1}{D^{'2}}}+\frac{1}{L_1C_1\|C_2}} \quad (4)$$

$$Q_2 = \frac{R}{\omega_{02}(L_1+L_2)\frac{C_1\omega_{01}^2}{C_2\omega_{02}^2}} \quad (5)$$

The transfer function of the chosen lead lag compensator $H_V\ (S)$ is [15] expressed in equation (6)

$$= \frac{S+\frac{1}{R_2C_2}}{R_1(C_2+C_3)S\left(S+\frac{1}{R_2(C_2\|C_3)}\right)} \quad (6)$$

$$= K_m\frac{(S+\omega_z)}{(S+\omega_p)} \quad (7)$$

$$K_m = \frac{1}{R_1(C_2+C_3)} \quad (8)$$

$$\omega_z = \frac{1}{C_2} \quad (9)$$

$$\omega_p = \frac{1}{R_2(C_2\|C_3)} \quad (10)$$

It attempts to stabilize the unstable ω_p in a stretch to achieve the designed closed loop performance through a pole zero compensation technique.

The overall transfer function seen in equation (11) is obtained by multiplying expression (6) with (1).

$$\frac{V_0}{V_C} = \frac{K_m\left(1+\frac{S}{\omega Z}\right)}{S\left(1+\frac{S}{\omega_{Pl}}\right)}\frac{1}{D^{'2}}\frac{\left(1-\frac{SL_1D^2}{RD^{'2}}\right)\left(1-\frac{SC_1\ (L_1+L_2)RD^{'2}}{L_1D^2}+\frac{S^2L_2C_1}{D}\right)}{\left(1+\frac{S}{\omega_{01}Q_1}+\frac{S^2}{\omega_{01}^2}\right)\left(1+\frac{S}{\omega_{02}Q_2}+\frac{S^2}{\omega_{02}^2}\right)} \quad (11)$$

Where ω_{Pl} angle of frequency at which the poles oscillate.

5. Simulation Results

The series SEPIC small signal model constructed using IGBT switches together with the lead lag compensator is simulated on a MATLAB – SIMULINK platform. The specifications of the parameters in the buck/boost converter system are $R_1 = 0.1\Omega$, $L_1 = 100\ \mu H$, $R_2 = 0.2\Omega$, $L_2 = 100\ \mu H$, $R_1 = 3e\text{-}3\ \Omega$ $C_1 = 680\ \mu F$, $R_0 = 1e\text{-}3\ \Omega$, $C_0 = 2200\ \mu F$. The system is designed to offer a stable output of 230 V from an input of 350 V when it operates as a buck converter and 350 V from an available input of 230 V in the boost mode.

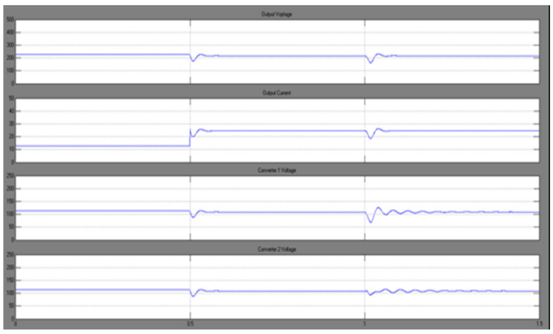

Fig. 3 Steady state and transient response of buck mode

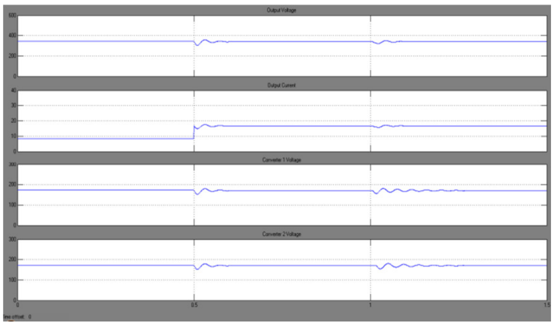

Fig. 4 Steady state and transient response of boost mode

The waveforms seen in Figs. 3 and 4 relate to the steady state and transient response when the series connected SEPIC is subjected to a load of 3 KW in both the buck and boost modes respectively. The mechanism allows the load voltage to be regulated, the individual converter voltages to be equally shared and the output current to reach its steady state value almost instantaneously in spite of sudden rises in load and supply at t= 0.5 and 1secs.The load current increases in tune with the increase in load and is accompanied by a marginal fall in voltage in both the modes as observed from the same figures. However the compensator endeavours to enable the load voltage to regain the desired value and the current to settle at its new value.

6. Stability Analysis

The ability to analyze engineering designs of power converters and associated controls is essential before proceeding to the engineering prototype phase. The analytical modelling of converters appear to make significant progress owing allegiance to the use of more accurate mathematical approaches, faster processing from personal computers, and availability of better tools. Among the several ways to determine the stability of dc-dcconverter, well known techniques are Bode, Nyquist, and root-locus plots and apply to nonlinear circuits with linearizing approximations.

The root locus is a way of presenting graphical information about a system's behaviour when the controller is working. The root locus is a widely used tool in the design of closed loop systems and finds its role to suit the stable operation of continuous time systems. It facilitates to locate the poles and zeros that move around in the S-plane for every value of gain through the use of simple rules. The time domain plots presented in Figs. 5,7 and 6, 8 establish the compensatory action in bringing the Eigen values from the right to the left half at 3 KW operating load for buck and boost SEPICs respectively.

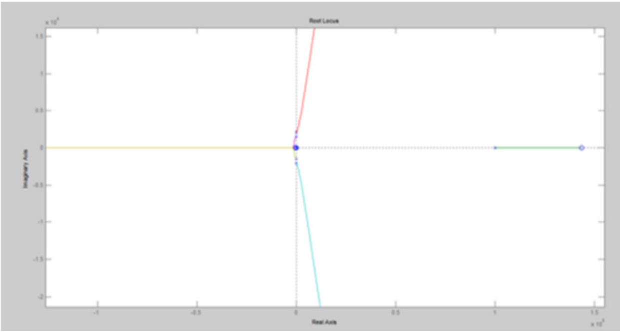

Fig. 5 Root locus of buck mode (unstable)

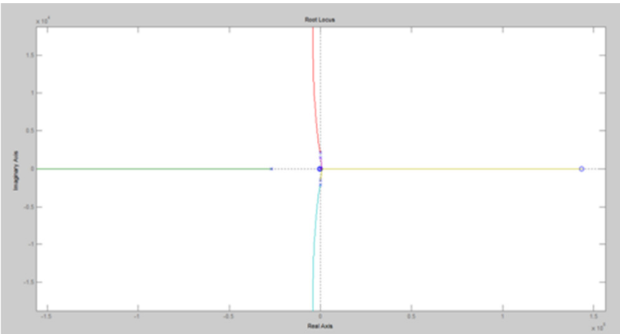

Fig. 6 Root locus of buck mode (stable)

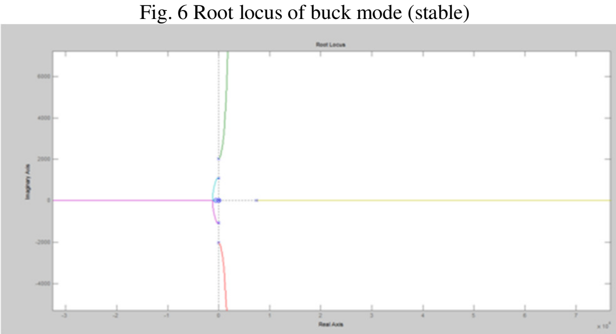

Fig. 7 Root locus of boost mode (unstable)

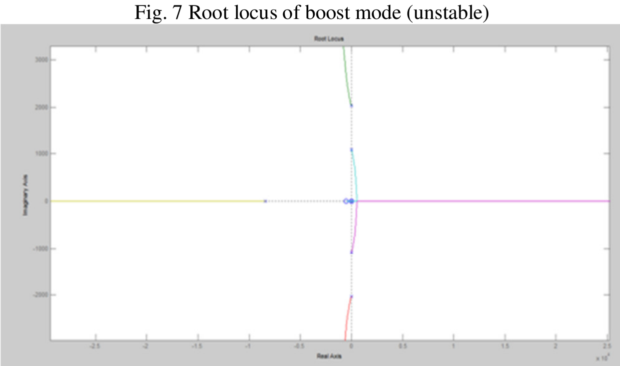

Fig. 8 Root locus of Boost mode (stable)

The Bode plot is a pictorial representation of the frequency response characteristics of the system and involves a graph of the system transfer function on a log-frequency axis. The stability is assessed by calculating the amplitude and phase angle for the transfer function and expressed as a measure of the gain and phase margins. The lead lag compensator illustrates its capability to extricate positive phase and gain margins at the same 3 KW load to elucidate the frequency domain stability of the converter system in both buck and boost trade offs as seen from Figs 9 through 12.

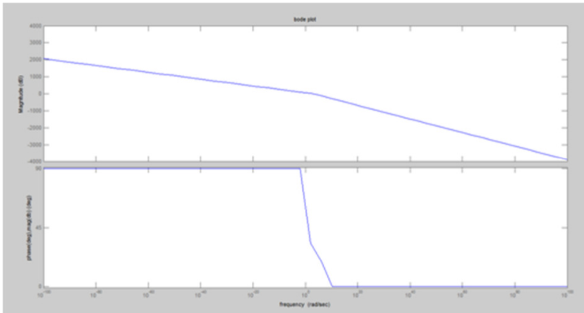

Fig. 9. Bode plot response of buck mode (unstable)

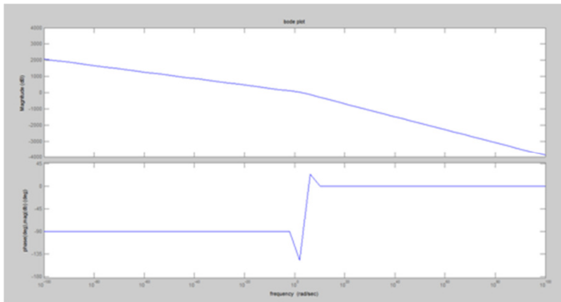

Fig. 10. Bode plot response of buck mode (stable)

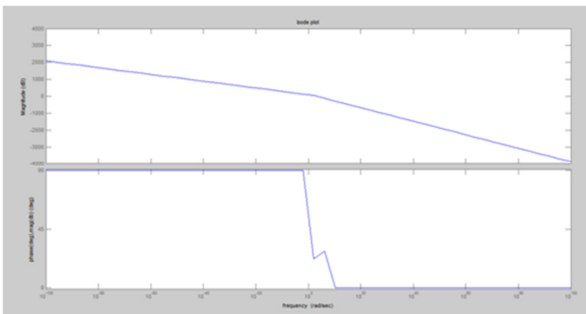

Fig. 11. Bode plot response of boost mode (unstable)

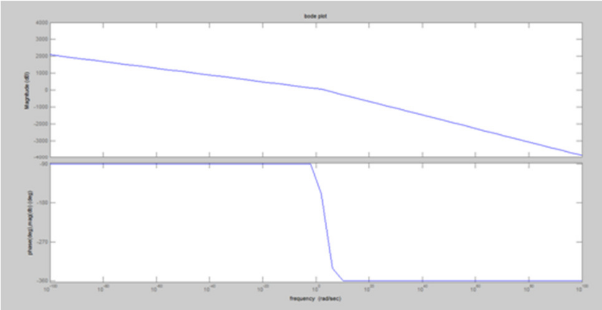

Fig. 12 Bode plot response of boost mode (stable)

Table 1. SEPIC BUCK

Power (KW)	Load current (A)		Converter 1 Voltage (V)		Converter 2 Voltage (V)		Output voltage (V)	
	Open loop	Closed loop	Open loop	Closed loop	Open loop	Closed loop	Open loop	Closed loop
1	2.65	4.32	190.00	115.60	190.04	115.60	380.10	231.62
2	5.53	8.67	181.40	115.40	181.38	115.40	362.70	230.77
3	8.59	13.10	174.70	114.52	174.85	114.52	349.40	229.04
4	12.88	17.48	155.25	114.45	155.20	114.45	310.25	228.84
5	17.75	21.98	140.86	113.72	140.80	113.72	281.73	227.45

Table 2. SEPIC BOOST

Power (KW)	Load current (A)		Converter 1 Voltage (V)		Converter 2 Voltage (V)		Output voltage (V)	
	Open loop	Closed loop	Open loop	Closed loop	Open loop	Closed loop	Open loop	Closed loop
1	2.08	2.84	240.00	175.90	240.52	175.90	480.00	351.79
2	4.32	5.70	231.45	175.42	231.43	175.42	462.80	350.83
3	8.57	8.57	174.98	175.02	174.95	175.02	349.95	350.05
4	12.58	11.45	158.95	174.73	158.90	174.73	317.90	349.45
5	17.67	14.32	141.50	174.48	141.48	174.48	283.00	348.95

The load current, individual converter voltages and the load voltage over varied values of load powers are seen in Tables 1 and 2 for buck and boost operating status respectively. It is observed that the feedback methodology introduced using the compensator enables the series connected topology to enjoy a balanced voltage at the output of each converter and a regulated load voltage across the range of operating loads.

6. Conclusion

The steady state stability of a series connected SEPIC system has been investigated through the use of its small signal model both in the time and frequency domains. A suitable lead lag compensator has been included to shift the eigen values of the characteristic equation to the left half of the S-plane. The root locus plot has been found to validate the proposed formulation and exhibit the stable operation. The acceptable phase and gain margins obtained from the bode plot have been found to add strength to the efficacy of the approach. The closed loop performance has been found to illustrate the viability of the scheme to suit the range of operating loads and elicit a higher scope for the use of SEPICs connected in series.

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