A Proposed OEIC Circuit with Two Metal Layer Silicon Waveguide and Low Power Photonic Receiver Circuit

Shiraz Afzal [*] **M. Zamin Ali Khan** [**] **Hussain Saleem** [***]

[*] **Electronics Engineering Department,**
Sir Syed University of Engineering & Technology, Karachi, Pakistan

[**] **Department of Main Communications Network,**
University of Karachi, Karachi, Pakistan

[***] **Department of Computer Science,**
University of Karachi, Karachi, Pakistan

Abstract

The recent developments in the field of optical communication have increased the need for Opto-Electronic Integrated Circuit (OEIC) used for the high speed data transmission with low power consumption, high bandwidth and compact size. Our research presents the OEIC chip with two metal layer waveguide and low power receiver circuit using standard CMOS technology. The silicon dioxide waveguide is composed of two metal layers, which is reducing metal layers to make OEIC cost effective. The silicon LED is fabricated using *n*-well/*p*-substrate with p^+ octagonal rings. The p^+/*n*-well forms the series *pn* junction to increase the light emitting area which operates in reverse bias mode. Photo detector is made of multiple *pn* junctions to increase the depletion region width with n^+ active implantation/*n*-well fabricated on the *p*-substrate. The photocurrent receiver circuit is made up of MOSFET to perform the function of photo detection and pre-amplification.

Keywords: *Opto Electronics, Silicon Waveguide, Photonic Receiver, Communication Electronics.*

1. Introduction

With the development in the field of electronic telecommunication, the silicon based photo emission & detection is becoming a vital zone in the optical communication for the next generation electronics. The OEIC chips play an important role to achieve high speed data transmission with high bandwidth, low power consumption and reduced interface noises making the chip very prevalent. The noise problems and the *RC* time delays associated with the electrical interconnections causing the urgent need of optical communication and with the emergence of OEIC chips placed us one step ahead in the field of optical communication.

In order to make OEIC chip cost effective, the silicon technology with two metal layers is proposed and to prevent dead layer associated with p^+ diffusion/*n*-well in the photodiode as the fact was reported by [1], n^+ diffusion/*n*-well on *p*-substrate photodiode is proposed. Earlier the OEIC chip with four metal layers with MOSFET receiver and p^+/*n*-well photodiode was reported by [2]. Unfortunately in this OEIC chip the p^+ diffusion in the photodiode origins the dead layer existence and thus in response to the light, it does not generate significant photocurrent as was early reported by [1]. Further improvement is made to brand the OEIC cost effective with two metal layer waveguide, utilizing silicon technology is proposed. The silicon technology is still the most feasible technology available in this regard. In this paper the proposed OEIC consists of LED as light emitting device and the photodiode as the light detecting device, two metal layer silicon waveguide and MOSFET receiver circuit.

With the introduction in the section-1, a detailed description about the principle of operations is explored in section-2. The paper is concluded in section-3.

2. Principle of Operations

Attributable to the imperative requirement of the light emitting device being compatible with the standard CMOS technology, abundant developments have been made in the field of silicon optical emitter. The *SiGe* Hetro-Structures, Nano-Crystals, Porous Silicon, Silicon Super Lattices, Erbium in Silicon, and Dislocation Engineering etc. are such methods but all approaches are not up to the mark and are unable to follow the CMOS technology standards.

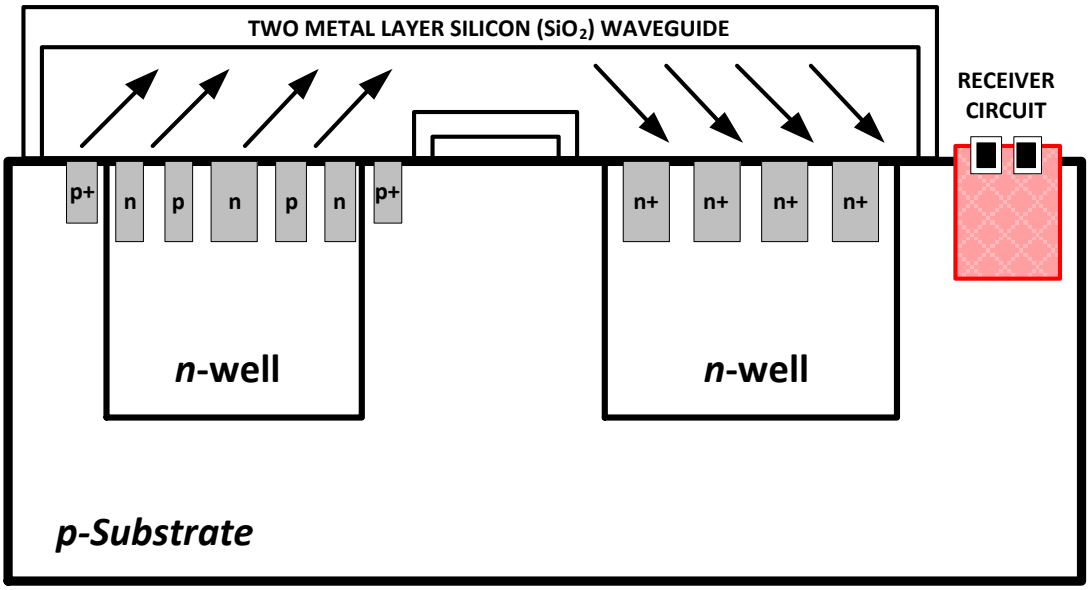

Figure-1: LED fabrication with photodiode and waveguide
using standard 0.35µm CMOS technology

The light emitting device that is used here is operated in "reverse-bias" mode to produce avalanche effect causing the operation above the breakdown voltage. According to [3] it operates silicon *PN* junction in reverse-bias setting, and making the light emission visible. A massive progress has been made in integrating the silicon LED on chip complying the standard VLSI technology [4][5][6]. In this paper, the LED is fabricated with photodiode and waveguide using standard 0.35μm CMOS technology. The fabrication sketch is presented in Fig-1.

The left hand side of the figure illustrates the fabrication of LED. It consists of inter-digital n^+ and p^+ octagonal rings con-centrically arranged around the *n*-center. Here the n^+ octagonal ring is used to reduce the breakdown voltage of the device while p^+/*n*-well forms the series of *PN* junction so as to increase the light emitting area. To prevent the diffusive carrier, p^+ protective ring is provided.

Due to this phenomenon, the multiplication of carrier takes place generating the avalanche effect since the reverse-bias voltage is applied across p+n interface which is equal to the threshold voltage. Therefore the electron and hole re-combination takes place causing the emission of visible light. The essential factor which is presented in this paper is the responsitivity of photodiode. The responsitivity is directly proportional to the width of the depletion layer due to the reason of having multiple *PN* junctions in the integration of photodiode.

In photodiode an interdigitated n^+ diffusion branch the fabrication inside the *n*-well and *p*-substrate from the anode. This interdigitated structure is employed to broaden the depletion layer and p^+ diffusion layer causing the existence of dead layer which is prevented by implementing the n^+ diffusion layer inside *n*-well. In order to increase the sensitivity of the *n*-well/*p*-substrate, the photodiode is made deeper inside the substrate. The existence of the potential barrier occurs due to the non-uniform doping profile [7]. Two potential barrier exist: (1) one is due to the non-uniformity and (2) another is due to the depletion of the donor from surface of the device. Significantly, in our proposed photodiode, this potential barrier is small. There is no potential barrier exist in the region between the fingers. On the other hand if p^+ diffusion layer is implemented, then this potential barrier would be large enough to cause presence of dead layer on the surface of the device. Therefore the responsitivity $R(\lambda)$ is given by the Eq.(1):

$$R(\lambda) = \frac{q\eta(\lambda)}{h\nu} T(\lambda) \left\{ \frac{W}{W+D} \left[s \int_0^{XD} e(-\alpha(\lambda)x)dx + \int_{XD}^{XB} e(-\alpha(\lambda)x)dx \right] + \frac{D}{W+D} \left[(1-c) \int_0^{XB} e(-\alpha(\lambda)x)dx \right] \right\} \quad \ldots(1)$$

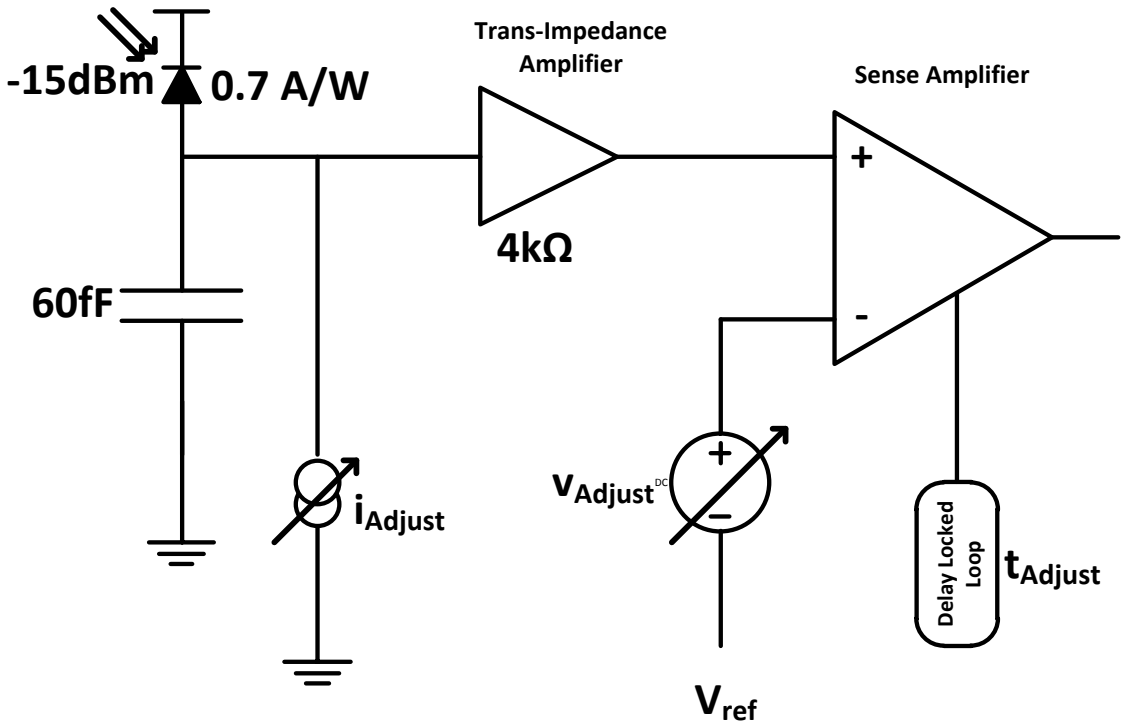

Figure-2: Low Power Receiver Circuit

Where,

q : charge of an electron,
η : internal quantum efficiency,
h : Planck's constant,
ν : frequency of the photon,
T : surface transmission coefficient,
W : width of the fingers,
D : distance between fingers,
s : percentage of minority carriers absorbed in the dead layer,
α : absorption coefficient,
X_j : potential barrier depth of the *n*-well,
X_l : dead layer width,
c : percentage of generated carriers between stripes that do not reach the anode.

Since, here we are taking "n^+ diffusion finger", therefore the dead width will be equal to zero so the Eq.(1) changes to:

$$R(\lambda) = \frac{q\eta(\lambda)}{h\nu} T(\lambda) \left\{ \frac{W}{W+D} \left[s \int_0^{XB} e(-\alpha(\lambda)x)dx \right] + \frac{D}{W+D} \left[(1-c) \int_0^{XB} e(-\alpha(\lambda)x)dx \right] \right\} \quad \ldots(2)$$

Hence the responsitivity equals to:

$$R = \eta \frac{q\lambda}{hc} \quad \ldots(3)$$

$$R = \frac{q\lambda}{hc}(1-R_f)\left(1 - \frac{e-\alpha w}{1+\alpha L}\right) \quad \ldots(4)$$

This formula in Eq.(3) & (4) shows clearly that responsitivity is directly proportional to the depletion layer width as reported in [2] where the author proposed four metal layers silicon waveguide. By using the two *PN* junction photodiodes as it is done in our proposed model, we have implemented the waveguide by reducing the two metal layers therefore we have to increase the responsitivity of photodiode approximately twice because by reducing the waveguide width the light intensity will be reduced so we have to increase the depletion layer width almost twice. In this regard, we have proposed four PN junction photodiodes here.

The waveguide in the proposed structure of OEIC is implemented using ultra large scale CMOS process. Therefore the waveguide using silicon dioxide which is implemented here is a planner process that makes it difficult to form step shape ridge waveguide. In order to resolve this problem CMOS technology with multiple layers of copper and silicon dioxide as an insulator is implemented. Moreover the receiver circuit presented in this paper which is used to extract the photocurrent is the low-power receiver [8] as depicted in Figure-2. The low-

power receiver circuit is made up of the trans-impedance amplifier (TIA), sense amplifier (SA) and delay locked loop (DLL). The input photo current is converted to small signal voltage by means of trans-impedance amplifier. Here the sense amplifier compares the input with the threshold voltage level to determine whether the data is 0 or 1. As shown in the Figure-2, the receiver has an option to adjust the input current level so that input voltage swings around the preset threshold voltage. The sense amplifier is triggered by the clock, therefore a clock-phase recovery circuit based on the delay locked loop is provided. The input sensitivity is -15dBm and the photodiode responsitivity is 0.7A/W.

3. Conclusion

The OEIC circuit with two metal layer waveguide and low power receiver circuit are designed and fabricated using CMOS technology. Here a new photodetector and receiver structure is optimized for the detection and amplification of photocurrent. The research scope can be extended by introducing new material like *GaN* that would be extremely valuable for high frequency applications.

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Shiraz Afzal is a full time faculty member of SSUET. He received his B.E. degree in Electronics from Sir Syed University of Engineering and Technology Karachi, Pakistan and M.E degree in Electronics, specialization in Micro-System design from NED University of Engineering & Technology Karachi, Pakistan in 2006 and 2012 respectively. His research interest includes Microelectronic circuit design. He is also a member of PEC.

Dr. M. Zamin Ali Khan is a Head of Main Communication network department at University of Karachi. He has received B.E. (Electrical Engineering) from NED University, Karachi, Pakistan and MS (Electrical & Computer Engineering) from Concordia University, Montreal, Canada and PhD in Computer Science from University of Karachi. He has more than 18 years of experience of teaching and industry. He has worked in Victhom Human Bionics, Canada as an Engineer Scientist. Currently. He is a senior member of Pakistan Engineering Council, Canadian Engineering Council and IEEE. His research interest includes VLSI, Digital design, Digital signal processing and Analog front end of wireless devices.

Hussain Saleem is currently Assistant Professor and Ph.D. Research Scholar at Department of Computer Science, University of Karachi, Pakistan. He received B.S. in Electronics Engineering from Sir Syed University of Engineering & Technology, Karachi in 1997 and has done Masters in Computer Science from University of Karachi in 2001. He has also obtained Diploma in Statistics. With having vast experience of about 15 years of University Teaching, Administration and Research in various dimensions of Computer Science, Hussain is the Founder member cum Pioneer of High Speed Fiber-based LAN Establishment Project with wireless computing support at University of Karachi, which became the largest campus network of Asia. He is also founder member of the Main Communication Networks Department, University of Karachi. Moreover, he is Academic Head of Computer Application Compulsory courses at Faculty of Arts and Sciences at University of Karachi. He is the Author of several International Journal publications. His field of interest is Software Science, System Automation, Hardware design engineering, and Simulation & Modeling. He is member of Pakistan Engineering Council (PEC).