Design of an energy-efficient CNFET Full Adder Cell

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Abstract

In this paper by using the carbon nanotube field effect transistor (CNFET), which is a promising alternative for the MOSFET transistor, two novel energy-efficient Full Adders are proposed. The proposed Full Adders show full swing logic and strong output drivability. The first design uses eight transistors and nine capacitors and the second design utilizes three capacitors less than the first design. Simulations, carried out using HSPICE based on the Stanford University CNFET model at 0.6V and 0.9V supply voltages, demonstrate the efficiency of type proposed circuit parameters such as delay, power and power-delay product.

Keywords: *Full Adder, Carbon NanoTube, CNFET, high performance, low power, Nanoelectronic.*

1. Introduction

As one of the major part of the arithmetic unit, Full Adders have a crucial role in speed and power consumption of the *VLSI* systems, because the Full Adders are used in most of the calculative and non-calculative applications. For instance, calculative operations such as multiplying, division and subtraction are performed by full adders and even for producing the memory address, Full Adders are used. As a result, designing a Full Adder with low power consumption, high speed operation and capability of producing a couple of *SUM-Cout* functions is of great important.

Formerly, the most efficient full adders have been designed using CMOS technology. However, as the dimensions decreased to nano ranges, designing digital circuits using CMOS technology faced many difficulties such as leakage current in short channel nanometer transistors. It has several types, such as reverse biased diode leakage, subthreshold leakage, gate oxide tunneling current, hot carrier gate current, gate induced drain leakage and channel punch-through current [1-4]. For instance, as the gate oxide tunneling current have reverse relation with gate oxide thickness, the thickness of dioxide can be increased, but this will lead to a decrease in the gate capacitor and consequently reduce the drain current, which leads to less driving and longer delay. In addition, more concern for changing and controlling *Vt* (threshold voltage) is also required in recent designs. However, changing *Vt* in *CMOS* technology is not easy. These challenges lead the researchers towards working on the emerging technologies such as Quantum-dot Cellular Automata (*QCA*), Nanowire transistors and Carbon Nanotube Field Effect Transistors (CNFET) as the substitutions for the conventional CMOS technology [5].

CNFET is the most appropriate successor technology for the classical *CMOS* technology among the other technologies, because *CNFET* transistors have similar functions to the *CMOS* transistors and I-V characteristics of *CNFET* transistors are like *CMOS* transistor. As a result, all of the designed infrastructures of the *CMOS* technology like *DPL*, *CAP-Inverter*, *CCMOS*, *Bridge CMOS* and etc. can be utilized again. Moreover, *Vt* in *n* and *p* transistors can be easily changed in *CNFET* technology and in contrast with *CMOS* technology difficulties about the diversities of the holes and electrons mobility are not concerned since the hole and electrons are relocated through a ballistic movement in carbon tube.

In this paper we present two high speed Full Adders which have been designed based on majority not function using *CNFET* technology. In the prototype we have used nine capacitors and six transistors and in the second type we have reduced the number of the capacitors to six .we simulate both of the proposed designs with HSPICE based on 32nm-*CNFET* technology at *0.6V* and 0.9V and compare delay, power consumption and power-delay product parameters with [1] and [2] which are the high-performance and low-power *CNFET*-based Full Adders, previously proposed in the literature.

2. CNTFET

Carbon NanoTube Field Effect Transistors (*CNFETs*) use semi conducting single wall carbon nanotube as transistor channel. Two types of *CNFET*, based on connection between *SWCNT* and source/drain of transistor are presented. If a *SWCNT* directly contact to source and drain of transistor, Schottky barrier transistor is created in their junction. The disadvantage of *SBCNFET*s is that I_{on}/I_{off} ratio is low. MOSFET like *CNFET* is another type of *CNFET* which unlike *SBCNFET* exhibit ambipolar behaviors. This type of *CNFET* is doped in un-gated

portions and behaves like *MOSFET* transistor. *MOSFET* like *CNFET*s have good characteristic such as; scalability compared to *SBCNFET*, reduced off leakage current and high current in source to channel junction in absence of Schottky barrier [6].

Depending on the angle of atom in tube, *SWCNFET* can act as conductor or semiconductor. This property which is determined with the chirality vector is represented by integer pair (N_1, N_2). Diameter of *SWCNT* with this vector is calculated using the following formula:

$$D_{CNT} = \frac{\alpha\sqrt{N_1 + N_2 + N_1 N_2}}{\pi} \quad (1)$$

Where α is the lattice constant equal to 2.49Å.
Threshold voltage is the voltage required to turn transistor on. Threshold voltage of *CNFET* transistors is dependent on diameter of *SWCNT* that is used in channel of transistor [7]. The *CNFET* threshold can be calculated by Eq. (2) below.

$$V_{TH} = \frac{0.42}{D_{CNT}(nm)} v \quad (2)$$

Our design is based on *MOSFET*-like *CNFET,* so in this paper we use the term *CNFET* instead of *MOSFET*-like *CNFET*.

3. Previous Works

There are some implementations of various full-adder cell designs in literature which are used for comparison in this paper. In [8] two high speed full adders based on majority function were presented, where *carryout* is implemented by three input majority function. Eq. (3) shows the basic idea behind this design.

$$Cout = \overline{Majority}(a,b,c) \quad (3)$$

Also in their design the *SUM* output, is implemented by means of five input *majority* function. The idea behind this implementation is exhibited in Eq. (4):

$$\begin{aligned} SUM &= \overline{Majority}(a,b,c,\overline{Cout},\overline{Cout}) \\ SUM &= abc + \overline{Cout}(ab+ac+bc) + \overline{Cout}(a+b+c) \\ SUM &= abc + \overline{Cout}.Cout + \overline{Cout}(a+b+c) \\ SUM &= abc + (\overline{ab}.\overline{ac}.\overline{bc})(a+b+c) \\ SUM &= abc + \overline{a}\overline{b}c + \overline{a}b\overline{c} \end{aligned} \quad (4)$$

Because there is no difference between producing *SUM* and *Cout* and their invert $(\overline{SUM},\overline{Cout})$, for ease of the implementation and increasing the performance, two *majority* functions were used to produce $\overline{SUM}$ and $\overline{Cout}$ instead of *SUM* and *Cout*. The first design is constructed in two stages.

In the first stage $\overline{Cout}$ is implemented by means of *majority-not* (*minority*) function and in the second stage they utilize 5 input *majority-not* function to implement $\overline{SUM}$. Two inputs of this five input *majority-not* gate were created by using the first stage output and the other three inputs, similar to first stage, are *a, b and c*.
First design has two disadvantages:

1. Using resistors in its pull up network results in having static power when n-CNFETs are on.
2. Non full swing characteristic due to employing resistors.

Their second design overcomes these problems by substituting the pull up resistor with p-*CNFET*. Second design is slower than the first one because of using p-*CNFET* in its pull up network, but it consumes less power and has a better PDP compared with the first design.
Figure 1 shows second design.

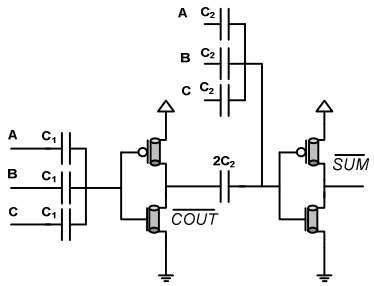

Fig.1 Presented resistor-free full adders in [8]

Another *CNFET* based full adder which is presented in [9] has eight transistors and eight capacitors. The basic idea of these designs is shown in Eq. (5).

$$SUM = Minority(a,b,c,2\times Nand(a,b,c),2\times Nor(a,b,c))$$

$$SUM = \overline{a}\overline{b}c + \overline{a}b\overline{c} + a\overline{b}\overline{c} + abc \quad (5)$$

Minority function, *Nand* and *Nor* Gate are implemented as presented in figure 2. In order to implement the minority function, an inverter with high-v_{th} for both *NCNFET* and *PCNFET* is used. For implementing *Nand* gate high-v_{th} *NCNFET* and low-v_{th} *PCNFET* and for modeling the *Nor* gate low-v_{th} *NCNFET* and high-v_{th} *PCNFET* are employed. This design has better characteristic compared with [8] in the terms of delay and power delay product, however utilizing eight capacitors influence the performance of the whole circuit as mentioned for the previous design [8]. Figure 3 shows the optimized proposed circuit [9].

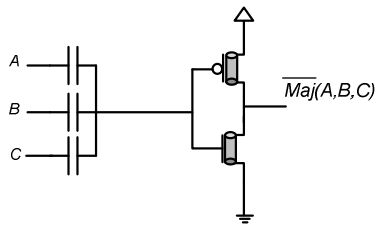

Fig.2 Majority not Function

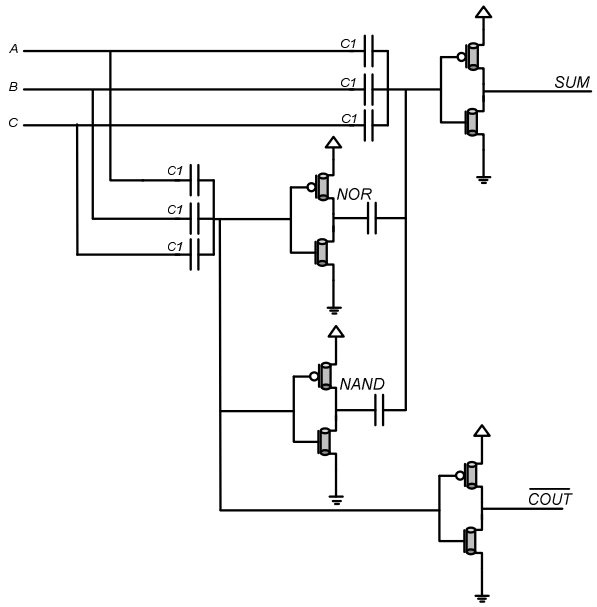

Fig.3 Presented full adder in [9]

Nonetheless we propose solutions to the problems of these full adders and our work has good characteristic in terms of speed, delay and power delay product as mentioned in [8] and [9].

4. The proposed Full Adder Cell

The proposed Full Adder cells are implemented by one *Minority*, *Nand* and *Nor* function, based on carbon nanotube technology. For implementing *Nand* gate with high- v_{th} *NMOS* and low- v_{th} *PMOS*, and for *Nor* gate low-v_{th} *NMOS* and high-v_{th} *PMOS* are used, this design also is based on the idea that the *Cout* function is the same as 3-input *majority*, we also achieved *SUM* with using a *minority* gate where its inputs is 3 input *Nand* gate, 3 input *Nor* gate and 3 input majority gate permanently. Followed formula is shown wherethrough a *Nand* and a *Nor* gate with one *Minority* function calculate the *SUM*.

$$SUM = \overline{Majority}(Nand(a,b,c), Nor(a,b,c), Majority(a,b,c))$$

$$SUM = Minority(Nand(a,b,c), Nor(a,b,c), (ab+ac+bc))$$

$$SUM = \overline{Nand}(a,b,c).\overline{Nor}(a,b,c) + \overline{Nand}(a,b,c).\overline{(ab+ac+bc)} + \overline{Nor}(a,b,c)\overline{(ab+ac+bc)}$$

$$SUM = (abc)(a+b+c) + (abc)(\bar{a}\bar{b} + \bar{a}\bar{c} + \bar{b}\bar{c} + \bar{a}\bar{b}\bar{c}) + (a+b+c)(\bar{a}\bar{b} + \bar{a}\bar{c} + \bar{b}\bar{c} + \bar{a}\bar{b}\bar{c})$$

$$SUM = \bar{a}\bar{b}c + \bar{a}b\bar{c} + a\bar{b}\bar{c} + abc \quad (6)$$

Table 1: Truth table of component of proposed circuit presented as below.

a	*b*	*c*	*Nand(a,b,c)*	*Nor(a,b,c)*	*Majority(a,b,c)*	*Majority(Nand(a,b,c),Nor(a,b,c),Majority(a,b,c))*	*SUM*
0	0	0	1	1	0	1	0
0	0	1	1	0	0	0	1
0	1	0	1	0	0	0	1
0	1	1	1	0	1	1	0
1	0	0	1	0	0	0	1
1	0	1	1	0	1	1	0
1	1	0	1	0	1	1	0
1	1	1	0	0	1	0	1

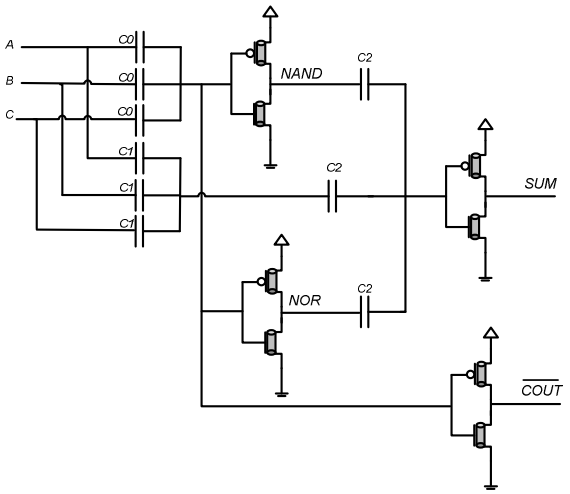

Fig.4 Design I

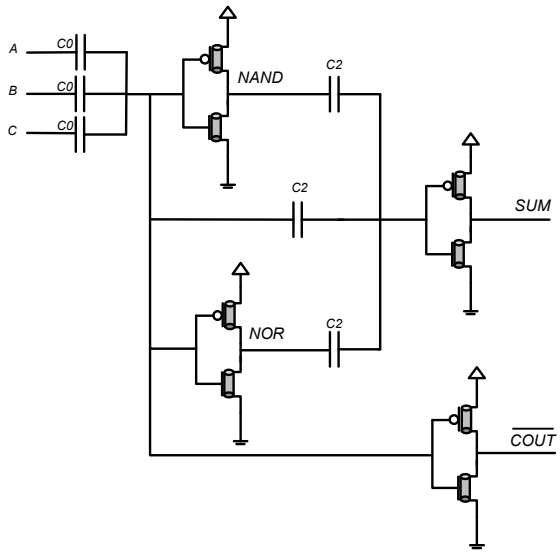

Fig.5 Design II

SUM is calculated in two steps, in the first step result of 3 input *Nand* and *Nor* gate along with majority outcome is achieved. In last step consequence result of first step used by a 3 input minority gate to obtain slightly result. The *Cout* signal also obtains with a *majority gate*. Figure 4 illustrate the proposed first full adder cell. The path which contain three parallel capacitors c_1 and serial by c_2 capacitor perform role of a three input majority gate. In figure 5 second proposed full adder cell is shown. Unlike the first design, input of *Nand*, *Nor* and c_2 is achieved from same three capacitors.

The proof of rectitude of proposed full adder cell is demonstrated as bellow:

In these equations, $c_i\mathrm{S}c_j$ and $c_i\mathrm{P}c_j$ denotes the equivalent series and parallel capacitance of c_i and c_j capacitors respectively.

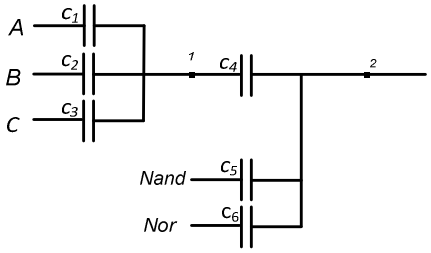

Fig.6 Circuit of proposed full adder

Three inputs are zero:

$$c_1 = c_2 = c_3 = 10ff$$

$$c_4 = c_5 = c_6 = 1ff$$

$$if\,(a=0,b=0,c=0) \Rightarrow$$

$$\begin{cases} c_1\mathrm{P}c_2\mathrm{P}c_3 \Rightarrow c_{q_1} = c_{q_{c_1,c_2,c_3}} = c_1 + c_2 + c_3 = 30ff \\ \left.\begin{matrix} Nand = 0.6 \\ Nor = 0.6 \end{matrix}\right\} c_5\mathrm{P}c_6 \Rightarrow c_{q_2} = c_{q_{c_5,c_6}} = c_5 + c_6 = 2ff \end{cases}$$

$$c_{q_3} = c_{q_1}Sc_4 \Rightarrow \frac{1}{c_{q_3}} = \frac{1}{30} + \frac{1}{1} \Rightarrow c_{q_3} = \frac{30}{31}ff$$

$$V_2 = \frac{2}{\frac{30}{31}+2} \times \frac{6}{10} \Rightarrow V_2 = 0.4$$

$$V_{out} = 0.4\rangle \frac{1}{2}vdd \Rightarrow v_{out} = 0 \qquad (7)$$

One of three inputs is one and two other are zero:

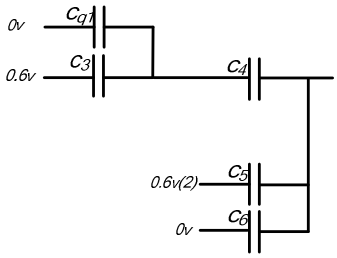

Fig.7 Circuit of proposed full adder with low voltage inputs

$$if\,(a=0,b=0,c=1)$$

$$c_{q_1} = c_1\mathrm{P}c_2 = c_1 + c_2 = 20ff$$

$$c_5\mathrm{P}c_6 \Rightarrow c_{q_2} = c_{q_{c_5,c_6}} = c_5 + c_6 = 2ff$$

$$c_{q_3} = c_{q_2}Sc_4 \Rightarrow c_{q_3} = \frac{2}{3}ff$$

$$c_{q_4} = c_{q_3}\mathrm{P}c_{q_1} \Rightarrow C_{q_4} = 20 + \frac{2}{3} = \frac{62}{3}ff$$

$$v_1 = \frac{10}{\frac{62}{3}+10} \times \frac{6}{10} \Rightarrow v_1 = 0.06$$

$$v_2 = \frac{1}{2+1} \times \frac{6}{100} \Rightarrow v_2 = 0.006 \qquad (8)$$

In second situation

$$c_{q_2} = c_3\mathrm{P}c_{q_1} \Rightarrow c_{q_2} = 30ff$$

$$c_{q_3} = c_{q_2}Sc_4 \Rightarrow c_{q_3} = \frac{30}{31}ff$$

$$c_{q_4} = c_{q_3} \mathrm{P} c_6 \Rightarrow c_{q_4} = \frac{61}{31} ff$$
$$v_2 = \frac{1}{\frac{61}{31}+1} \times \frac{6}{10} \Rightarrow v_2 = \frac{186}{920} \quad (9)$$

Super potion:

$$v_2 = \frac{186}{920} + \frac{6}{100} \langle \frac{1}{2} vdd \Rightarrow v_{out} = 1 \quad (10)$$

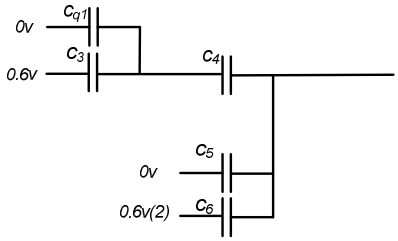

Fig. 8 Circuit of proposed full adder with only one high voltage input

$$if\,(a=0, b=1, c=1)$$
$$c_{q_1} = c_2 \mathrm{P} c_3 \Rightarrow c_{q_1} = 20 ff \quad (11)$$

Based on superposition property:
In first situation,

$$c_{q_2} = c_5 \mathrm{P} c_6 \Rightarrow c_{q_2} = 2 ff$$
$$c_{q_3} = c_4 S c_{q_2} \Rightarrow c_{q_3} = \frac{2}{3} ff$$
$$c_{q_4} = c_{q_3} S c_1 \Rightarrow c_{q_4} = \frac{10}{16} ff$$
$$v_1 = \frac{20}{\frac{10}{16}+20} \times \frac{6}{10} \Rightarrow v_1 = 0.581$$
$$v_2 = \frac{1}{1+2} \times 0.581 \Rightarrow v_2 = 0.193 \quad (12)$$

In second situation

$$c_{q_2} = c_1 \mathrm{P} c_{q_2} \Rightarrow c_{q_2} = 30 ff$$
$$c_{q_2} = c_4 S c_{q_2} \Rightarrow c_{q_3} = \frac{30}{31} ff$$
$$c_{q_4} = c_{q_2} \mathrm{P} c_5 \Rightarrow c_{q_4} = \frac{61}{31} ff$$
$$v_2 = \frac{1}{\frac{61}{31}+1} \times \frac{6}{10} \Rightarrow v_2 = 0.202 \quad (13)$$

Based on superposition property

$$v_2 = 0.202 + 0.193 \rangle \frac{1}{2} vdd \Rightarrow v_{out} = 0 \quad (14)$$

And three inputs are on:

$$if\,(a=0.6, b=0.6, c=0.6) \Rightarrow$$
$$\left.\begin{array}{l} c_{q_1} = c_1 \mathrm{P} c_2 \mathrm{P} c_3 \Rightarrow c_{q_1} = 30 ff \\ Nand = 0 \\ Nor = 0 \end{array}\right\} \Rightarrow c_{q_2} = c_5 \mathrm{P} c_6 \Rightarrow c_{q_2} = 2 ff$$
$$c_{q_3} = c_{q_1} S c_4 \Rightarrow c_{q_3} = \frac{30}{31} ff$$
$$v_2 = \frac{\frac{30}{31}}{\frac{30}{31}+2} + \frac{6}{10} \Rightarrow v_2 = 0.195$$
$$v_2 = 0.195 \langle \frac{1}{2} vdd \Rightarrow v_{out} = 1 \quad (15)$$

6. Simulation and comparison

A compact model of CNFETs based circuit simulation has been presented in [10]. In this model MOS-CNFET device is implemented in three levels. In the first level the intrinsic behavior of MOS-CNFET has been modeled, in second level the non-idealities of device have been included and finally in the third level multiple CNTs for each MOS-CNFET device are acceptable. In this paper third level is used for simulation the CNFET based circuit. Supply voltage 0.6 and 0.9 in two frequencies 100 and 250 MHz are used for simulating all of the circuit at room temperature. Because in [9] the carry-out was generated as $\overline{Cout}$ and in [8] both of the *SUM* and *Cout* were generated as $\overline{SUM}$ and $\overline{Cout}$, for fair comparison, inverters are attached to these circuit. It has been a common practice to treat the full-adder cell as a standalone cell in simulation [11-14]. It is also not unusual that the full-adder cells which perform well in standalone situation, fail upon actual deployment because of the lack of driving power. This is because full-adder cells are normally cascaded to form a useful arithmetic circuit. Therefore, the full-adder cells must possess sufficient drivability to provide the next cell [15]. All the required input-pattern-to-input-pattern transitions are included in the test patterns. The power

consumption and delay are measured for the third cell. Comparison of full adders is discussed below in three subsection; delay, power, PDP.

6.1 Delay comparison: For each transition, delay is measured from 50% of the input voltage swing to 50% of the output voltage swing. The maximum delay is taken as the cell delay. Our design has short critical path for generating Sum and COUT and has the smallest delay among the existing full adder. Table IV depicts the full adder cells delay in 0.6 and 0.9 *v* voltages and in two frequencies, 100 and 250MHz.

Table 2: Delay comparison of full adder cells

Delay	***Frequency 100***		***Frequency 250***	
Design\Voltage	*.6*	*.9*	*.6*	*.9*
[8]	*2.99E-10*	*1.05E-10*	*2.74E-10*	*1.02E-10*
[9]	*1.52E-10*	*3.13E-11*	*1.52E-10*	*1.52E-10*
Design I	*4.88E-10*	*2.41E-10*	*4.83E-10*	*2.41E-10*
Design II	*2.05E-10*	*1.25E-10*	*2.03E-10*	*1.25E-10*

6.2 Power comparison: The average power dissipation has been evaluated by applying casual pattern. Also no short-circuit current occur during the -operation of the circuit. Table V shows power consumption of full adder cells in 0.6 and 0.9 v voltages and in two frequencies, 100 and 250MHz.

Table 3: Power comparison of full adder cells

Power comparison	***Frequency 100***		***Frequency 250***	
Design\Voltage	*.6*	*.9*	*.6*	*.9*
[8]	*9.74E-07*	*1.85E-05*	*1.15E-06*	*2.08E-05*
[9]	*1.94E-06*	*4.67E-05*	*1.94E-06*	*2.22E-05*
Design I	*1.50E-06*	*9.60E-06*	*1.73E-06*	*9.60E-06*
Design II	*1.02E-06*	*2.49E-05*	*1.20E-06*	*2.53E-05*

6.3 Power-Delay-Product comparison: The PDP is a quantitative measure of the efficiency and a compromise between power dissipation and speed. PDP is particularly important when low power operation is needed. Table VI present PDP of full adder cells in 0.6 and 0.9 v voltage and in two frequencies, 100 and 250 MHz.

Table 4: Power-Delay-Product comparison of full adder cells

Power-Delay-Product comparison	***Frequency 100***		***Frequency 250***	
Design\Voltage	*.6*	*.9*	*.6*	*.9*
[8]	*7.33E-16*	*1.95E-15*	*3.14E-16*	*2.13E-15*
[9]	*2.95E-16*	*1.46E-15*	*2.95E-16*	*3.38E-16*
Design I	*7.34E-16*	*2.31E-15*	*8.34E-16*	*2.31E-15*
Design II	*2.10E-16*	*3.10E-15*	*2.44E-16*	*3.15E-15*

7. Conclusion

This paper presented a new improved design of full adder cell with considerable improvement in power and delay, compared to the latest design of full adder cell in 4 different states that made by two different frequencies and to different supply mode. The number of transistor of presented full adder not only reduced number of transistors that were employed in full adder cell but also improve the size of adder and multiplayer cell in VLSI design.

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