A Fault-tolerant 32 nm CMOS Double Sideband Amplitude Suppressed Carrier Modulator-Demodulator Circuit Implementation

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Abstract

This paper presents a low-voltage, low-power and fault-tolerant implementation of Double Sideband Suppressed Carrier (DSB-SC) amplitude modulator-demodulator circuit for portable communication systems. Through the approximation proposed in this work, a CMOS four quadrant multiplier is used as a (de)modulator circuit to generate DSB-SC (de)modulated signals. Furthermore, the proposed fault-tolerant modem can be used to enhance the reliability of safety-critical communication systems since it is able to provide duplicated output using two path output computations. The proposed circuit occupies a small surface area and is functional at high frequencies even with a low supply voltage. SPICE simulations of the post-layout extracted CMOS multiplier in a full-custom 32 nm CMOS technology, which include all parasitic, are used to demonstrate the electrical behavior of the circuit.

Keywords: *DSB-SC, Modulator, Demodulator, Fault tolerance, Four Quadrant Multiplier, 32nm CMOS technology.*

1. Introduction

Modulation is the process by which a high frequency sine wave signal (i.e., the carrier) is modified in accordance with a baseband voice, video, or digital message signal (i.e., the modulating signal) to be transmitted. The modified carrier signal is called the modulated signal. To be specific, the carrier can be modified through amplitude modulation, frequency modulation, or phase modulation. Many types in amplitude modulation, for example, Double-Sideband Suppressed Carrier Modulation (DSB-SC), have been proposed with different advantages, disadvantages, and practical applications [1-2]. A consequence of modulation is the translation of the message spectrum to a higher frequency band while the demodulation is the process which extracts the message signal from the modulated signal [1-2].

In the modulation process, modulators have been used to generate modulated signals. Among modulators, the simplest modulator is the multiplier modulator. In literature, there are several approaches to design multipliers, each with different operating speed, power consumption, and circuit complexity. The simplest electronic multiplier circuits use logarithmic amplifiers. However, this type of multiplication has very limited bandwidth and single quadrant operation. A far better type of multiplier uses the Gilbert Cell which was invented by Barrie Gilbert in the late 1960s [3].

Due to the increasing demand for portable electronics for communications and other applications, circuit systems are now required to have a longer battery life and a lower weight [4-5]. Thus, the need for portable electronic equipments has pushed the industry to produce high-speed circuit systems with a very low voltage power supply. In addition, the continuous growth of integration densities in Complementary Metal-Oxide-Semiconductor (CMOS) technology has driven the rapid growth of very large scale integrated (VLSI) circuits for today's electronics industries [6]. Thus, circuit systems with new CMOS process technologies can operate at higher frequencies with less power. For these reasons, the CMOS process has been considered as the most suitable process technology for communication circuits [5].
However, with the introduction of nano-scale CMOS technologies, analog and mixed designers are now faced with many new challenges at different phases of design. As technology advances to deep sub-micron levels and below, VLSI circuits increase in complexity and become more susceptible to process variations that induce parameter variations in VLSI circuits [7-8]. Due to these parameter variations in VLSI circuits, transient and permanent faults arise; and these problems can engender data corruption. Thus, for communication systems with safety-critical applications, fault-tolerant

designs are required so that the designed system can perform safety-critical functions accurately. [9].

In general, fault tolerance of circuit systems can be improved through hardware or software approaches. However, communication systems are usually real-time systems. In other words, in most cases, we cannot predict the nature of transmitted/received signals. Therefore, fault-tolerant hardware design approaches seem to be best suited in analog communication systems. For real-time applications, the correspondent safety level needs to detect and correct failures that arise during normal operation. Therefore, we can employ Concurrent Error Detection (CED) techniques. Among different CED techniques, the most basic method is hardware redundancy. In hardware redundancy, two copies of the hardware are used concurrently to perform the same computation on the same data. At the end of each computation, the results are compared and any discrepancy is reported as an error [10]. For example, in output duplication based CED technique the output of a circuit can be monitored by a checker. In other words, if an error causes violation of the property, the checker gives an error indication signal [11-12].

In this paper, the implementation of a fault-tolerant DSB-SC Amplitude Modulator-Demodulator circuit with high speed, low voltage, low power and small-size capabilities is presented. Through the proposed design approximation presented in section 3, a CMOS four quadrant multiplier, which has two outputs, is used as a modem to generate DSB-SC modulated and demodulated signals [13]. Furthermore, the CMOS four-quadrant multiplier circuit is able to generate duplicated outputs using two path output computations which ensure its ability of fault tolerance.

The multiplier is simulated in full-custom 32 nm CMOS technology. The circuit presented in this work occupies only a small surface area, which is ideal for portable communication systems. Furthermore, the circuit is functional at high frequencies even with a supply voltage V_{DD} equal to 0.3V. Therefore, it can be used to reduce the power consumption and prolong a longer battery life for portable systems.
The organization of this manuscript is as follows: the proposed (de)modulation technique is first presented in Section 2, followed by the DSB-SC (de)modulator CMOS four-quadrant circuit multiplier analysis in Section 3. Finally, the (de)modulator simulation results and the circuit's fault analysis with all parasitic are respectively illustrated in Section 4 and section 5.

2. The Fault-tolerant Double Sideband Amplitude Modulation-Demodulation Technique

2.1 The Typical Analog Communication System

The general block diagram of a typical analog communication system [2] is given by Fig. 1.

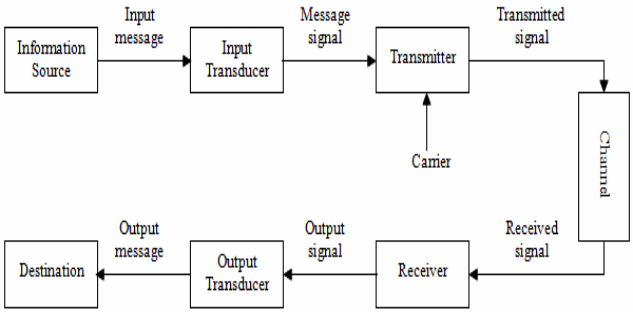

Fig. 1 A typical Analog communication system block diagram.

The typical communication system given by Fig. 1 includes an input transducer that converts the input message produced by the information source into a signal that is encoded and transmitted over an adapted communication channel and converted (decoded) by the receiver into an output signal. Finally, the output transducer converts the reconstructed output signal into an output message which is the message received by the destination [1-2].

To gain better understanding of the modulation-demodulation process, an analog communication system from the modulation-demodulation point of view [2] is given by Fig. 2. But, we should note that a modulator is only one of the blocks in a transmitter and similarly, a demodulator is just one part of the blocks in a receiver.

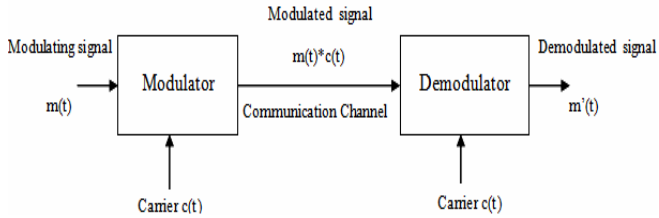

Fig. 2 Analog communication system from the modulation-demodulation point of view.

In AM modulation, transmission of carrier consumes a lot of power. Since, only the side bands contain the information about the message, carrier is suppressed and the result is the DSB-SC wave [2]. The DSB-SC signal or the modulated signal is obtained through multiplying the message signal to be transmitted (m(t)) with the carrier signal (c(t)) as shown in the modulator block diagram presented by Fig. 3.

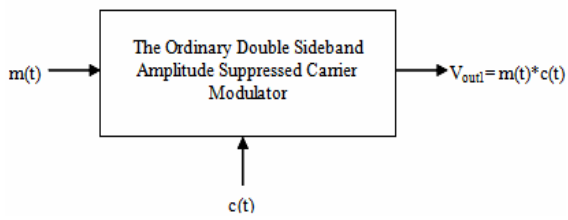

Fig. 3 The ordinary DSB-SC modulator block diagram

Hence, the baseband signal becomes a passband signal with frequency that is much larger than the maximum frequency in m(t) and can be easily transmitted using a relatively short antenna [2].

2.2 The Proposed Fault-Tolerant DSB-SC Amplitude Modulation Technique

The proposed fault-tolerant DSB-SC amplitude modulation technique is presented by the block diagram of Fig. 4.

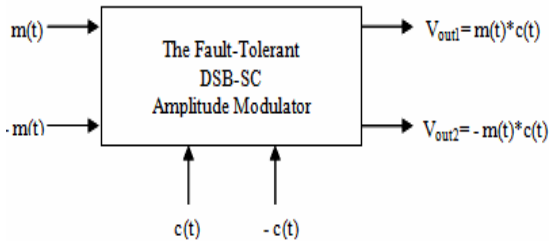

Fig.4 The fault-tolerant modulator block diagram

In the proposed DSB-SC modulation circuit, the fault-tolerance property is ensured by using a duplicated output computation based concurrent error detection method. In fact, this CED method is based on generating duplicated outputs using two path output computations. The first path gives the first modulated signal which is the output V_{out1} (m(t)*c(t)) and the second path gives the second modulated signal which is the output V_{out2} (-m(t)*c(t)). In other words, instead of transmitting only the message m(t), we will transmit the considered message and its opposite (m(t), -m(t)). In that way, when errors caused by faults occur, they will affect, in most cases, only one of the two paths. Consequently, one of the two transmitted message m(t) and -m(t) will be fault-free which will prevent data corruption.

In addition, by using duplicated calculation techniques we can perform the same function in two different ways. Thus, we can add a circuit checker that can detect the occurrence of errors by checking the properties of the outputs. In our case, for example, we can add a checker circuit to verify that V_{out2}=-V_{out1}. Hence, any violation of this property will immediately indicate a circuit malfunction. Therefore, in order to obtain the modulated signals V_{out1} and V_{out2} (m(t)*c(t), - m(t)*c(t)) we will use the message to be transmitted and its opposite (m(t), -m(t)) and similarly, the carrier signal and its opposite (c(t), -c(t)).

2.3 Demodulation of DSB-SC Signals

While modulation results in the baseband translation of the modulating signal spectrum to radio frequency band, the reverse process of translating the modulated signal spectrum back to the baseband to facilitate human perception is referred to as demodulation [2]. In Fig. 5, we show the schematic diagram of a DSB-SC demodulator.

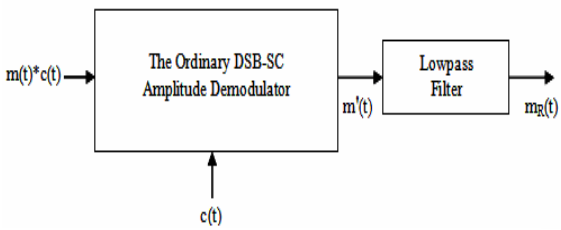

Fig.5 The ordinary DSB-SC demodulator block diagram

As shown in the above figure, the received modulated signal (DSB-SC signal) is multiplied in the receiver by a locally-generated carrier wave which is synchronous with the transmitted carrier. In fact, the locally transmitted carrier is assumed to be in phase with the transmitted carrier and having the same frequency. In order to eliminate the undesired high frequency terms, the resulting signal m'(t) obtained using the DSB-SC product multiplier is passed through a lowpass filter which has a cutoff frequency equal to the modulating signal frequency. If the demodulation is successful, m_R(t) the output of lowpass filter should be proportional to information message m(t). In fact, we should note that before multiplying the modulated signal by the locally generated carrier, the received signal can be passed through a band-pass filter centred at the carrier frequency in order to pass the DSBSC signal and eliminate any out-of-band noise.

2.4. The Proposed Fault-Tolerant DSB-SC Amplitude Demodulation Technique

The fault-tolerant DSB-SC demodulation technique is presented by the block diagram of Fig. 6.

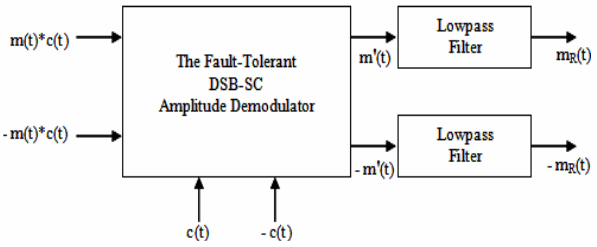

Fig.6 The fault-tolerant demodulator block diagram

As shown in Fig. 6, the proposed fault-tolerant DSB-SC demodulation technique is based on recuperating not only the original message signal m(t) but also its opposite –m(t). Actually, the demodulation process of a DSB-SC signal involves obtaining the original information signal m(t) or its scaled version from the two modulated signals. In fact, the received DSB-SC modulated signals (m(t)*c(t), - m(t)*c(t)) are respectively multiplied in the receiver by the locally-generated carrier wave and its opposite. The locally-generated carrier must be synchronous with the transmitted carrier. The resulting signals m'(t) and –m'(t) are then low-pass filtered to obtain the two information signals $m_R(t)$ and - $m_R(t)$. The multiplier circuit used to achieve the demodulation process could be similar to that used in the modulator.

3. The Four Quadrant Multiplier Circuit Analysis

"An analog multiplier is a device having two input ports and an output one. The signal at the output is the product of the two input signals. If both input and output signals are voltages, the transfer characteristic is the product of the two voltages divided by a scaling factor. Some of the circuits used to produce electronic multipliers are limited to signals of one polarity. If both signals are unipolar, we have a single quadrant multiplier, and the output will also be unipolar. If one of the signals is unipolar, but the other may have either polarity, the multiplier is a two-quadrant multiplier and the output may be bipolar. Finally, the four quadrant multiplication operation means that both inputs may be either positive or negative, as may be the output" [3].

In fact, there are several approaches to design CMOS multipliers, each with different operating speed, power consumption, and circuit complexity. Also, different multipliers based on different topologies such as V-I converters, differential amplifier, summing and squaring circuit, etc have been presented in literature [14]. This work presents a CMOS analog multiplier with low-voltage, low-power and small-size capabilities. The basic block diagram of four quadrant voltage mode multiplier [13] is shown in Fig. 7.

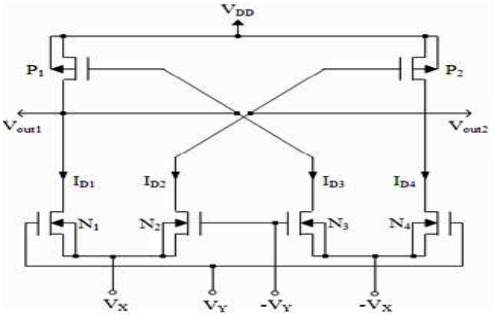

Fig.7 Basic circuit schema of the four quadrant analog multiplier

In the current four quadrant multiplier circuit, the PMOS transistors P_1, and P_2 operate in the saturation region, while the NMOS transistors N_1, N_2 N_3 and N_4 operate in the triode region. The drain current I_D of an NMOS transistor in the saturation and triode regions can be presented respectively as [15-16]:

$$I_D = K\left(V_{GS} - V_{Tn}\right)^2 \quad (1)$$

And

$$I_D = 2K\left[\left(V_{GS} - V_{Tn}\right)V_{DS} - \frac{V_{DS}^{\ 2}}{2}\right] \quad (2)$$

Where:

$$K = \frac{1}{2}K'\frac{W}{L}$$

$$K' = \mu_n C'_{ox}$$

K is the transconductance parameter that depends on the geometry of the transistor (the width/length ratio for the channel) and on K' which is fixed for a given technology and cannot be changed by the circuit designer. μ_n is the electron mobility, C_{OX} is the gate oxide capacitance per unit area, W/L is the transistor aspect ratio. V_{Tn} is the threshold voltage of the NMOS transistor. V_{DS} is the drain-to-source voltage and V_{GS} is the gate-to-source voltage [16].

Equation 1 presents the expression of the drain-source current for the NMOS transistor in its saturation region of operation. In this region, the current depends on the square of V_{GS}-V_{Tn} but it is independent of the drain-to-source voltage V_{DS}. The most important parameter of a MOS transistor is the dynamic transconductance g_m. In fact, g_m relates the change in the drain current to the change in the gate-to-source voltage at a constant value of V_{DD}. g_m is given by the next equation [16]:

$$g_m = \frac{dI_D}{dV_{GS}} \quad \text{at a constant value of } V_{DD} \quad (3)$$

Thus, to find the expression of g_m, we must find the derivative of the expression of the drain current I_D with respect to the gate-to-source voltage. Therefore, g_m is given as:

$$g_m = \frac{2K}{V_{GS} - V_{Tn}} \quad (4)$$

The dynamic transconductance can be also expressed as follows:

$$g_m = \frac{2I_D}{V_{GS} - V_{Tn}} \quad (5)$$

Therefore, the dynamic transconductances g_{mp1} and g_{mp2} respectively of the two PMOS transistors P1 and P2 are expressed as:

$$\begin{cases} g_{mp1} = \dfrac{2(I_{D1} + I_{D3})}{V_{OUT1} - V_{DD} - V_{Tp}} & (6) \\ g_{mp2} = \dfrac{2(I_{D2} + I_{D4})}{V_{OUT2} - V_{DD} - V_{Tp}} & (7) \end{cases}$$

As from Equations 6 and 7, we can obtain the following useful equation:

$$(I_{D2} + I_{D4}) - (I_{D1} + I_{D3}) = \frac{1}{2}\left(g_{mp2}V_{OUT2} - g_{mp1}V_{OUT1}\right) \quad (8)$$

Equation 2 presents the expression of the drain-to-source current for the NMOS transistor in its triode region of operation, in which a resistive channel directly connects the source and drain. This resistive connection will exist as long as the voltage across the oxide exceeds the threshold voltage at every point in the channel [16]. Thus Equation 2 is available only if $V_{GS} - V_{Tn} \geq V_{DS} \geq 0$.

For small drain-source voltages such that $\frac{V_{DS}}{2} << V_{GS} - V_{Tn}$ Equation 2 can be reduced to [16]:

$$I_D = \mu_n C'_{ox} \frac{W}{L}(V_{GS} - V_{Tn})V_{DS} \quad (9)$$

In equation 9, the current I_D through the MOSFET is directly proportional to the voltage V_{DS} across the MOSFET. Thus, the transistor behaves like a resistor connected between the drain and source terminals, but the resistor value can be controlled by the gate-to-source voltage.

From the basic circuit schema of the four quadrant analog multiplier presented in Fig. 7, we can extract the following expressions of the drain-to-source voltages and the gate-to-source voltages for the four NMOS transistors N_1, N_2, N_3 and N_4:

$$\begin{cases} V_{DS1} = V_{out1} - V_X \\ V_{DS2} = V_{out2} - V_X \\ V_{DS3} = V_{out1} + V_X \\ V_{DS4} = V_{out2} + V_X \end{cases} \quad And \quad \begin{cases} V_{GS1} = V_Y - V_X \\ V_{GS2} = -V_Y - V_X \\ V_{GS3} = -V_Y + V_X \\ V_{GS4} = V_Y + V_X \end{cases}$$

In Fig. 7, the Basic circuit schema of the four quadrant analog multiplier shows that the two gates of the N_1 and N_4 NMOS transistors are connected to the input V_Y while two gates of the N_2 and N_3 NMOS transistors are connected to the input ($-V_Y$). In this work, for each NMOS transistor, we will add a DC component V_{DC} to each gate-to-source voltage V_{GS}. Consequently, Equation 9 can be expressed as:

$$I_D = \mu_n C'_{ox} \frac{W}{L}(V_{GS} + V_{DC} - V_{Tn})V_{DS} \quad (10)$$

In addition, if we choose the DC component V_{DC} equal to the threshold voltage V_{Tn}, Equation 10 can be reduced to:

$$I_D = \mu_n C'_{ox} \frac{W}{L} V_{GS} V_{DS} \quad (11)$$

As from Equation 11, the drain current of each NMOS transistor can be expressed as:

$$\begin{cases} I_{D1} = K'V_{DS1}V_{GS1} \\ I_{D2} = K'V_{DS2}V_{GS2} \\ I_{D3} = K'V_{DS3}V_{GS3} \\ I_{D4} = K'V_{DS4}V_{GS4} \end{cases}$$

Then we have:

$$\begin{cases} I_{D1} + I_{D3} = 2K'\left(V_X{}^2 - V_X V_Y\right) \\ I_{D2} + I_{D4} = 2K'\left(V_X{}^2 + V_X V_Y\right) \end{cases}$$

Finally, we obtain the second useful equation:

$$(I_{D2} + I_{D4}) - (I_{D1} + I_{D3}) = 4K'V_X V_Y \quad (12)$$

As from Equations 8 we have:

$$(I_{D2} + I_{D4}) - (I_{D1} + I_{D3}) = \frac{1}{2}\left(g_{mp2}V_{OUT2} - g_{mp1}V_{OUT1}\right)$$

We obtain the following equation relating the outputs of the four quadrant circuit to its inputs:

$$g_{mp2}V_{OUT2} - g_{mp1}V_{OUT1} = 8K'V_X V_Y \quad (13)$$

Taking into consideration all the equations and approximations adopted in this section, the multiplier is designed and implemented in order to generate two opposite output signals V_{out1} and V_{out2} such as $V_{out2} = -V_{out1}$. Thus, the equations and approximations described in this section are used to design the fault-tolerant modulator-demodulator circuit in full custom 32nm CMOS technology at 0.3 V supply voltage [17]. Fig. 8 presents the layout of the (de)modulator circuit. It occupies only an area of 0.96×0.93µm2.

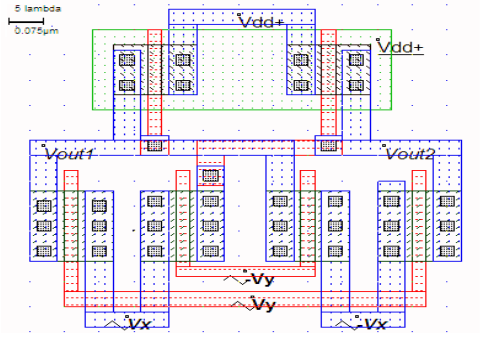

Fig. 8 Layout of the four quadrant multiplier circuit in full-custom 32 nm process technology

SPICE simulations of the post-layout extracted CMOS multiplier, which includes all parasitic, are used to demonstrate the acceptable electrical behaviour of the proposed fault-tolerant modulator-demodulator circuit.

4. The DSB-SC Modulator-Demodulator Circuit Simulation Results

4.1 The Modulator Simulation Results

The modulator is implemented using the CMOS four quadrant multiplier circuit presented in Fig. 8. To do so, the message signal m(t) and its opposite –m(t) are respectively connected to V_X and $-V_X$ the first inputs of the multiplier circuit. While the locally generated carrier c(t) and its opposite –c(t) are respectively connected to the inputs V_Y and $-V_Y$ of the multiplier circuit. The simulation results presented in this work are obtained using a sinusoidal signal message m(t) of 1000 MHz frequency and the locally generated carrier is a high frequency sinusoidal signal of 10 GHz. The time domain DSB-SC waveforms are illustrated in Fig. 9.

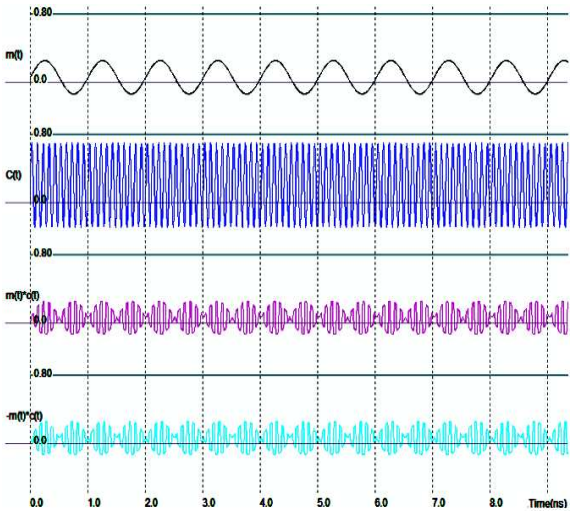

Fig.9 The fault-tolerant DSB-SC signals in the time domain

Fig. 10 presents the superposition of the two modulated signals m(t)*c(t) and –m(t)*c(t) in the time domain.

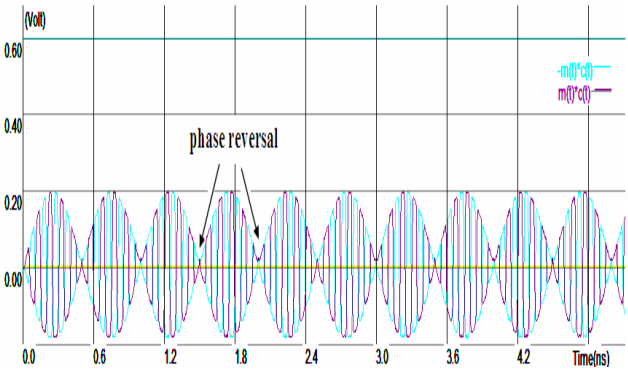

Fig.10 The two superposed DSB-SC modulated signals in the time domain

As indicated in the end of section 3, Fig. 10 shows that the four quadrant multiplier circuit implemented as a modulator product generates two opposite outputs which are the DSB-SC modulated signals m(t)*c(t) and -m(t)*c(t). In fact, the DSB-SC modulated signal is always accompanied by a phase-reversal. In Fig. 10, the two arrows indicate the points of carrier phase reversals for the two generated modulated signals. This phase reversal is typical of DSB-SC amplitude modulation. Carrier phase reversals in the DSB-SC signal occurs at the time instants where the modulating signal m(t) crosses zero [2].

In order to understand how frequency translation of the modulating signal takes place, we use the Fast Fourier Transform. Fig. 11 shows the spectrum of the modulating signal while Fig. 12 shows the spectrum of the DSB-SC modulated signal.

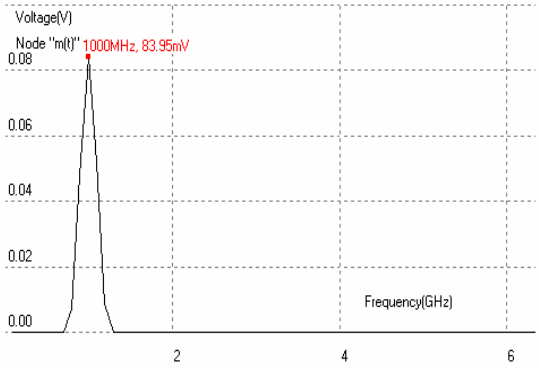

Fig.11 Spectrum of the message signal

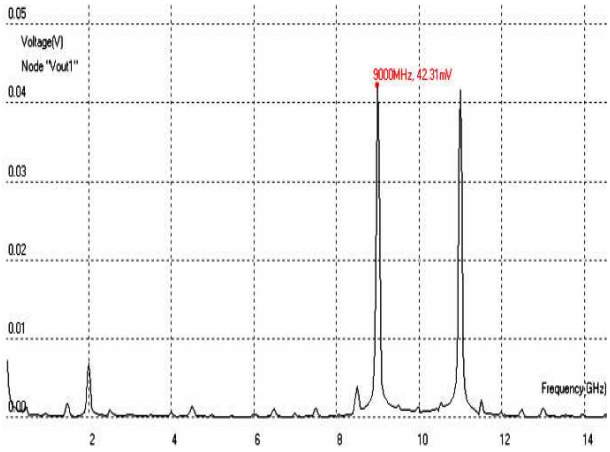

Fig. 12 Spectrum of the DSB-SC modulated signal

Fig. 12 presents the spectrum of the DSB-SC modulated signal. In fact, we notice that there is no pulse at the carrier frequency which is equal to 10 GHz. Thus, In DSB-SC modulation, the carrier signal is suppressed by the product modulator circuit and the modulated signal containing no carrier as shown in Fig. 12. Hence, the term suppressed carrier is employed because the transmitted signal does not have a discrete component at the carrier frequency [2]. Consequently, a great percentage of power that is dedicated to it is distributed between the sidebands. Hence, compared to AM and for the same used power, DSBSC signal can be reliably received at greater distances. As illustrated in Fig. 12, the spectrum presents two pulses respectively at (f_c-f_m) and (f_c+f_m) frequencies, where f_m is the frequency of the message signal and f_c is the frequency of the carrier signal. Thus, the fact that the modulated signal contains both portions of the spectrum explains why the term, double-sideband, is used [2]. The bandwidth of the modulated signal is twice as large as the bandwidth of the modulating signal which is equal to f_m. Thus, the bandwidth of the DSB-SC amplitude modulation is equal to 2 GHz.

4.2 The Demodulator Simulation Results

The demodulator is implemented using the same four quadrant multiplier circuit presented in Fig. 8. To achieve this, we connect the two received modulated signals m(t)*c(t) and -m(t)*c(t) respectively on V_X and $-V_X$ the first inputs of the multiplier circuit. As for the modulator, the locally generated carrier c(t) and its opposite –c(t) are respectively connected to the inputs V_Y and $-V_Y$ of the multiplier circuit. SPICE simulations of the post-layout extracted CMOS multiplier, which include all parasitic, are used to demonstrate the acceptable electrical behaviour of the proposed demodulator. The time domain of DSB-SC modulated and demodulated signals are illustrated in Fig. 13.

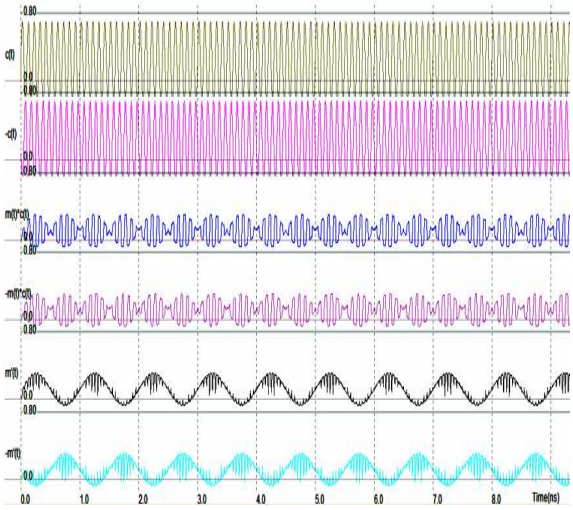

Fig.13 The fault-tolerant DSB-SC signals in the time domain

In Fig. 13, the two signals m'(t) and its opposite –m'(t) are the first and the second output of the demodulator product. Thus, m'(t) and –m'(t) must be low-pass filtered to obtain the desired transmitted information signals. Fig. 14 shows the spectrum of the DSB-SC demodulated signal resulting from the demodulator product.

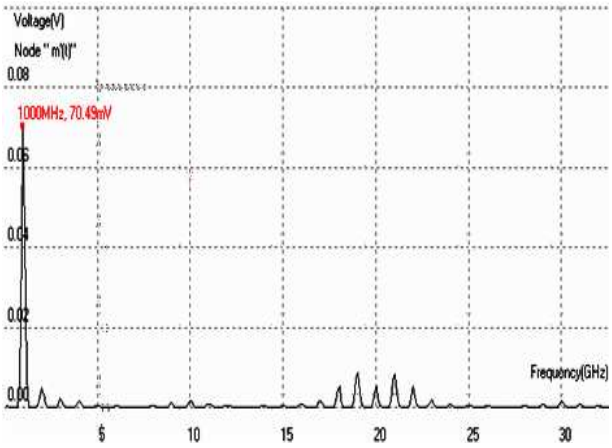

Fig. 14 Spectrum of the DSB-SC demodulated signals

As shown in Fig. 14, the spectrum presents two components, the first is the desired message signal and the second is a DSB-SC signal centred at 20 GHz ($2f_C$). By passing the signals resulting at the outputs of the demodulator product through a well-designed low pass filter, we will obtain two signals ($m_R(t)$ and $-m_R(t)$) which are proportional to the transmitted information message signal m(t) and its opposite –m(t).

5. The modulator-demodulator Circuit Fault Analysis

Due to the diversity of VLSI defects, it is hard to generate complementary tests for real defects. Therefore, fault models are necessary to analyse any VLSI circuits in the presence of faults. In the following sub-section, we analyse the behaviour of our fault-tolerant modulator-demodulator circuit with respect to the set of fault models including bridging and open faults. In fact, in analog CMOS technology, faults are further classified into catastrophic (open and bridging) and parametric faults. When a catastrophic defect occurs, the topology of the circuit is changed. In fact, a bridging defect is a short circuit between two or more nets on a die [18-19], while an open circuit defect can result from missing metal material in the transistor interconnects. To prove the efficiency of the proposed technique, the most likely faults of open and bridging circuit type are deliberately injected in the layout. In the following sections, we will inject some probable faults type single open defect in the layout of the modulator-demodulator circuit.

- **Fault 1**

The first fault injected and simulated is an open fault in the metal level connecting the two drains respectively of the two transistors P_1 and N_1 in the modulator product circuit. Fig. 15 gives the Electrical SPICE simulations results.

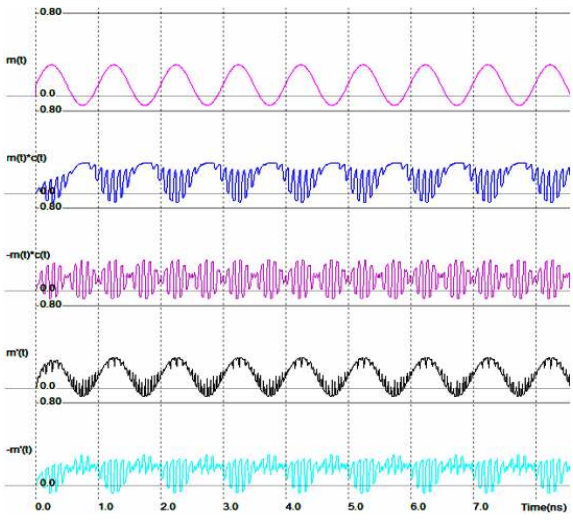

Fig.15 The fault-tolerant DSB-SC modulator-demodulator signals with injection of fault 1 in the time domain

From Fig. 15, we deduce that the injection of the open defect induces a faulty modulated signal m(t)*c(t) which is completely distorted. On the other hand, the open defect injection has no effect on the second output of the modulator which is the opposite of the modulated signal (-m(t)*c(t)). Consequently, the second output computation of the modulated signal has given a fault-free signal which prevents data corruption. Accordingly, the fault tolerance property is ensured for the DSB-SC modulator circuit.

Now, let us consider the effect of the injection of fault 1 in the DSB-SC demodulator product circuit. Fig. 15 shows that the injection of the considered fault in the transmitter (the modulator product circuit) has an effect on -m'(t) the second output of the demodulator circuit which is distorted while m'(t) the first output of the demodulator circuit is fault-free and once filtered using a low pass filter we will obtain the adequate desired information signal. Consequently, simulation results prove that fault tolerance property is ensured for the DSB-SC modulator-demodulator circuit.

- **Fault 2**

The second fault consists of injecting the same fault 1 in the circuit of the receiver. Thus, we will inject an open fault in the metal level connecting the two drains respectively of the two transistors P_1 and N_1 in the demodulator product circuit. Fig. 16 shows the simulation results the in presence of fault 2.

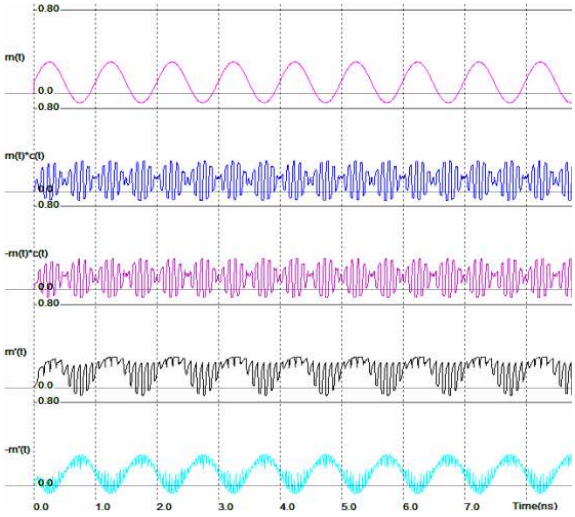

Fig. 16 The fault-tolerant DSB-SC modulator-demodulator signals with injection of fault 2 in the time domain

From Fig. 16, we notice that the two outputs of the modulator circuit are fault-free which is quite normal because the fault is injected into the demodulator circuit. On the other hand, m'(t) the first output of the demodulator circuit is distorted while its opposite –m'(t) is fault-free. Then, we prove again that the fault tolerance property is ensured for the considered DSB-SC modulator-demodulator circuit with respect to the open defect fault model. In the following sections, we will inject some probable faults type single short defect (bridging fault) in the layout of the modulator-demodulator circuit.

- **Fault 3**

The third fault simulated is a bridge connecting the drain and the source of the NMOS transistor N_2 in the modulator circuit. Fig. 17 gives the considered electrical SPICE simulations results.

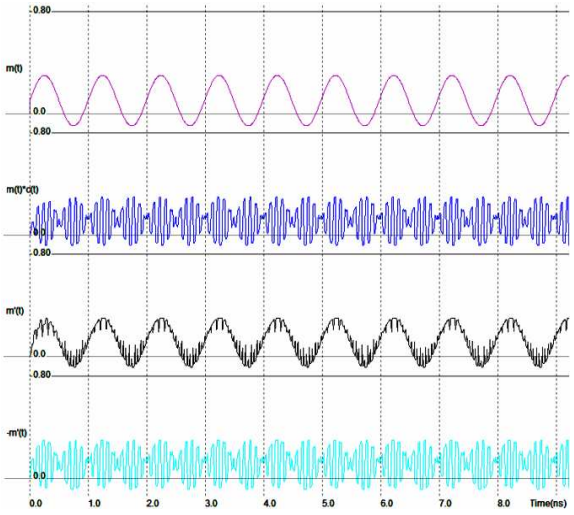

Fig.17 The fault-tolerant DSB-SC modulator-demodulator signals with injection of fault 3 in the time domain

In Fig. 17, we show that the injection of fault 3 has no effect on m'(t) the first output of the demodulator product while –m'(t) the second output of the demodulator corresponds to the modulated signal m(t)*c(t). Thus the fault-tolerance property is also ensured for the modulator-demodulator circuit with respect to the bridging fault model.

- **Fault 4**

The last fault injected is a bridge connecting the gate and the source of the NMOS transistor N_2 in the demodulator circuit. Due to fault 4, the second output of the demodulator is court-circuited with the common gate of the two transistors N_2 and N_3 on what we receive the opposite of the locally generated carrier. Fig. 18 gives the considered electrical SPICE simulations results.

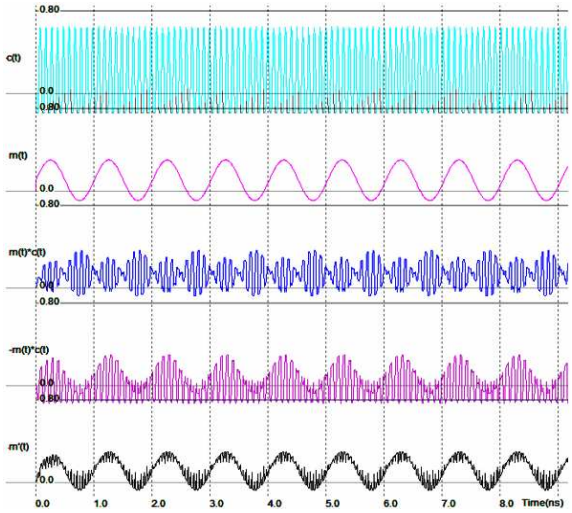

Fig.18 The fault-tolerant DSB-SC modulator-demodulator signals with injection of fault 2 in the time domain

The simulation results presented in Fig. 18 show that circuit has also tolerated the current bridging fault since the first output m'(t) of the demodulator circuit is fault-free. Thus the fault tolerance property is ensured for the DSB-SC modulator-demodulator circuit with respect to the single bridging fault model.

6. CONCLUSION

The expansion of wireless services and other telecom applications increases the need for low-cost mobile VLSI solutions with very demanding requirements including high speed, low power supply voltage and low power consumption. In this paper, the 32 nm CMOS technology node is used to implement a four-quadrant multiplier used as a fault-tolerant DSB-SC modulator-demodulator that can be used in high reliable communication systems. The implemented (de)modulator circuit that generates fault-tolerant DSB-SC signals can operate at high frequencies up to 10 GHz with power consumption equal to 50µW. The circuit is functional for very low supply voltage. In fact, the simulation results show that the circuit is functional even with a power supply voltage equal to 0.3V. Thus, simulation results show that the technique is effective and can easily be implemented in the System-on-Chip environment.

References

[1] Louis E. Frenzel Jr., "Principles of Electronic Communication Systems", Electronic Design Magazine, 3rd ed. chapter 3, 2008.
[2] T.G. Thomas and S.G. Sekhar, "Analog Communication", Tata McGraw-Hill Education, 2006.
[3] Hank Zumbahlen, "Linear Circuit Design Handbook", Elsevier-Newnes, ISBN-10: 0750687037, ISBN-13: 978-0750687034, 2008.

[4] S. S. Rajput and S. S. Jamuar, "Low voltage analog circuit design techniques,"IEEE Circuits and Systems Magazine, vol. 2, no. 1, pp. 24–42, First Quarter 2002.
[5] S. YA, N. Edgar and S. SINENCIO, "Low Voltage Analog Circuit Design Techniques:A Tutorial", IEICE Trans. Analog Integrated Circuits And Systems, VOL.E00–A, No.2, FEBRUARY 2000.
[6] M. Karmani, C. Khedhiri & B. Hamdi, "Design and test challenges in Nano-scale analog and mixed CMOS technology", International Journal of VLSI design & Communication Systems (VLSICS) Vol.2, No.2, 2011.
[7] M. Orshansky, S. R. "Nassif and D. Boning, Design for manufacturability and statistical design: A constructive approach", US Springer, 2008, pp. 1–8.
[8] R. Garg and S. P. Khatri "Analysis and Design of Resilient VLSI Circuits: Mitigating Soft Errors and Process Variations", US Springer, 2010, pp. 1-10.
[9] E. F. Hitt and D. Mulcar, "Fault-Tolerant Avionic", CRC Press LL, 2001.
[10] N. Joshi, K. Wu, J. Sundararajan, and R. Karri, "Concurrent Error Detection for Evolutional Functions with applications in Fault Tolerant Cryptographic Hardware Design", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 25, 2006, pp. 1163–1169.
[11] C. Zeng and E. J. McCluskey, "Finite State Machine Synthesis with Concurrent Error Detection", Proc. International Test Conference, 1999, pp. 672-679.
[12] M. Karmani, C. Khedhiri, B. Hamdi, K.L. Man, C. Lei and E.G. Lim, A Concurrent Error Detection Based Fault-Tolerant 32 nm XOR-XNOR Circuit Implementation, in Proceedings of the IAENG International MultiConference of Engineers and Computer Scientists - IMECS'12, Hong Kong, March, 2012.
[13] P. Srividya, KR. Rekha and K.R Nataraj, "VLSI Implementation of an Analog Multiplier for Modem", International Journal of Engineering Science and Technology (IJEST), Vol. 3 No. 2011.
[14] P. Mohan Kumar, "Low-Voltage CMOS Analog Multiplier", master thesis, Thapar University, July 2011.
[15] L. Shen-Juan and H. Yuh-Shyan, "CMOS Four-Quadrant Multiplier Using Bias Feedback Techniques", IEEE Journal of Solid-State Circuits, Vol.29, No.6, June 1994.
[16] R. Jacob Baker, "CMOS circuit design layout and simulation", IEEE Series on Microelectronics Systems, WILEY Publication, Third Edition, 2010, PP.140-145.
[17] E. Sicard, Microwind and Dsch version 3. 1, INSA Toulouse, ISBN 2-87649-050-1, Dec 2006.
[18] P. Marwedel, "Embedded System Design, Embedded Systems Foundations of Cyber-Physical Systems," Springer, 2nd Edition, 2011.
[19] L. S. Milor, "A tutorial introduction to research on analog and mixed-signal circuit testing," IEEE Trans. Circuits and System., vol. 45, pp.1389–1407, Oct. 1998.

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