Optimization of multi - channel HDLC protocol transceiver using Verilog

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Abstract

To transmit and receive data at high speed in any network without any error a protocol is required. HDLC protocol of layer-2 of OSI model which is most suitable for bit oriented packet transmission mode is discussed in this article. HDLC protocol was designed with two full-duplex channels on the principle of Top-Down design. Verilog HDL coding of the design is done using Xiliux ISE and is implemented on Vertex FPGA, The design has been verified through simulation and synthesis of the existing and proposed design.

Keywords: *FPGA, HDLC, Bit Synchronous and High Speed.*

1. Introduction

High-level data link control (HDLC) is a bit oriented data link protocol designed to support both half-duplex and full-duplex communication over point-to-point and multipoint links and switched and non switched channels. It is developed by International Organization for Standardization.

Another benefit of using this protocol is that the control information of the received or transmitted data is at same position and in specific bit pattern but differ from the data which reduces error.

HDLC Frame

The term "Frame" is used in HDLC to indicate an entity of data or an unit of data transmitted or received. Each frame starts and ends with a bit pattern 01111110 to indicate header and trailer of a particular frame sent. This bit pattern is called Flag of the frame as shown in the figure below.

Flag	Address	Control	Data	FCS	Flag

Figure1 HDLC Frame Structure

To differentiate flag from the data of the frame. If five consecutive 1s are found in data at transmitter data a zero is inserted so that it should not be read as flag at the receiver. If five consecutive 1s are received in the data on the receiver side next 0 bit which was intentionally inserted at the transmitter is eliminated so as to get the original data.

Address Field is used to identify the address of receivers. Control Field is further divided into Information Frame, Supervisory Frame and Unnumbered Frame. Data or Information field is used to transport data. FCS (Frame Checksum) field is used for error detection and correction.

2. System Description

The HDLC protocol transceiver consists of the following main blocks

- Control unit and Registers
- The Transmitter
- The Receiver

- Dual port RAMS and RAM management unit
- Interrupt Controller

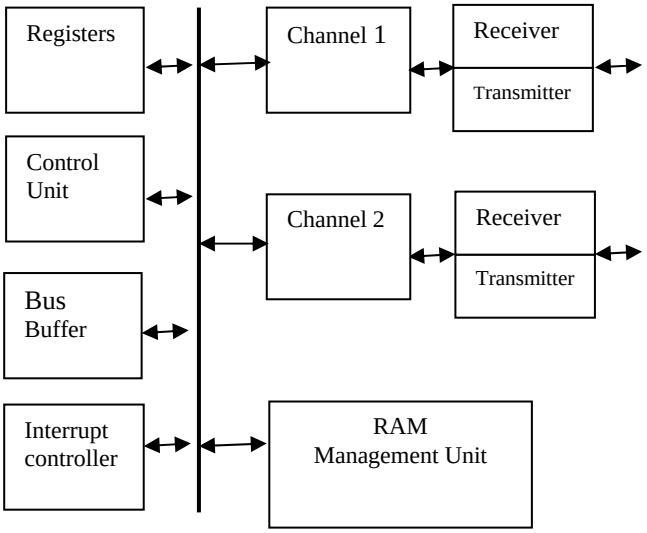

Fig. 2 Transceiver block diagram

2.1 Control unit and Registers

This unit is responsible to select whether data is to be transmitted or received or both and if transmitted then to select any one of the two channels channel-1 or channel-2 over which data is to be transmitted and give the address to the address field of the destination. If the system has to receive then select one of the two channels over which data has to be received. During reception this unit keeps an eye on incoming data to detect starting flag of the frame or bit pattern "01111110" when the flag is recognized it decodes the address field for its address to continue receiving data.

There are 16 registers in the chip which includes registers to hold frame during reception and transmission on channel 1 and channel 2, registers indicating status of the operation, registers to detect flag of the frame and register to check error using frame check sequence (FCS).

2.2 The Transmitter

Transmitter is responsible for inserting Flag in the beginning and end of frame, calculating CRC, bit stuffing, inserting address of the destination, inserting abort and idle sequence.

After the system is initialized when start signal is assert by the HDLC processor. It checks the command to transmit flag (01111110) which indicates start of the Frame. Station address is set by the HDLC processor which is stored in RAM and can be any arbitrary address or broadcast of "all-stations" address which are all ones. After the address field control bits are transmitted which are responsible for flow management and it indicates type of the frame being transmitted i.e. whether the frame is Supervisory, Unnumbered or Information frame. Usually data transmission is done by Information frame, other two are used Network management and flow control.

Data is transmitted after control bits, If there is a bit pattern "11111" found in the data an extra "0" is inserted after that to prevent this portion of data to be read as end of frame or ending flag "01111110". To transmit data without any error FCS is calculated along with the transmission of data. CRC shift register is a16-bit linear feedback shift register used for computing FCS which is a 16-bit Cyclic Redundancy Check.

Flag is transmitted again to mark end of frame. At any time during transmission when abort signal is assert by HDLC processor transmission of current frame is aborted by sending abort flag(01111111) .

HDLC transceiver is designed using Verilog HDL in Xilinx ISE design tool. The design is synthesized with Vertex FPGA as target device and its functional simulation is carried out using Modelism simulator.

2.3 Receiver

The main function of the receiver is to receive the frame whose address is same as the address of the receiver station; it also receives the frames holding common address for all stations.

When receive signal is assert by the HDLC processor receiver start searching for the flag (01111110) which indicates beginning of the incoming frame, once the flag has been detected it checks the address field of the frame to verify if the frame has been sent for this station or some other station .If the address of the frame is same as the address of the receiving station or it is common address for all stations to receive data it starts receiving rest of the frame to start with control field which indicates type of the incoming frame. CRC operation starts with data field to detect any error in the received data.

Receiver discards any "0" found after five "1s" which are intentionally inserted at the transmitter to prevent the receiver to read the bit pattern as end of frame or flag. After the whole data has been received CRC is calculated and stored in a register to compare it with the FCS field to be received after the data. If received and calculated CRC are same then "No Error" flag is set by the HDLC processor and if not then "Error" flag is set.

Another flag “01111110” ends the frame and receiver starts searching for the next flag to receive next frame.

Status Bits			Operation of HDLC Processor
Flag	TR/CH	TR/CH	
0	0	0	Channel 0 of Receiver Searches for Flag
0	0	1	Channel 1 of Receiver for Flag
0	1	0	Channel 0 of Transmitter Inserts Flag
0	1	1	Channel 1 of Transmitter Inserts Flag
1	0	0	Channel 0 of Receiver finds Flag and Start receiving Frame
1	0	1	Channel1 of Receiver finds Flag and Start receiving Frame
1	1	0	Channel 0 of Transmitter transmits frame
1	1	1	Channel 1Transmitter transmits frame

Table 1: Status Bits and Operation of HDLC processor

2.4 Interrupt Controller

An Interrupt requirement may come into being when either of the two channels finished transmitting or receiving. The interrupt status include if the operation is finished successfully and the error status such as FCS error or frame length. When all 1s or previous bits of frame is not properly sent due to some error in between transmitter or receiver which results interrupt to occur.

3. Design Results

HDLC transceiver is designed using Verilog HDL in Xilinx ISE design tool. The design is synthesized with Vertex FPGA as target device and its functional simulation is carried out using Modelsim simulator.

Device utilization for Vertex FPGA with speed grade -4 of present and proposed design is shown in table which clearly indicates that design proposed in this paper covers less chip area and the maximum operating frequency of this design is 70.64 Mhz. which is nearly double of the previous which operated on 40Mhz.

Device Utilization						Maximum Operating Frequency	
Resource	Available	Used					
		Present Design		Proposed Design		Present Design	Proposed Design
4 input LUTs	1536	854	55%	31	2%	40Mhz.	70.64Mhz
IOBs	98	51	52%	12	12 %		
Slice Flip Flops	1536	610	39%	33	2%		

Table 2:Comparison of FPGA Resource and Speed of the two design methods

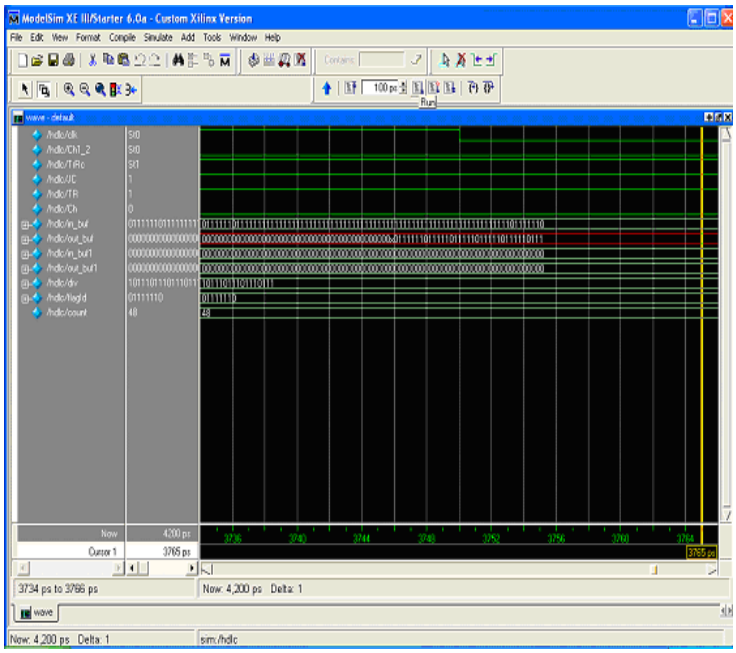

Figure 3: Simulation results of HDLC Transceiver sending data in channel 1

Simulation results of HDLC Transceiver are shown in the above figure in which data from input buffer is being transferred to output buffer after verification of flag in the beginning of the frame. As shown in the figure bit stuffing is being done as data is transferred to output buffer. FCS is also calculated and its result has to be sent within the frame so as to be compared at the receiver end to detect if there is any error in the received data.

4. Conclusions

In this project, HDLC protocol transceiver with double full duplex channels has been successfully implemented in

Xilinx ISE with Vertex FPGA as target. We have designed a multi-channel high speed HDLC processor. The results of device utilization and maximum operating frequency are then compared with the previous designs of Single channel and Multi-channel HDLC controller and it is observed that this design has covered less chip area and is faster as compared to the previous one.

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