A Differential Double Pass Transistor Logic Unit

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Abstract

In this paper we present a new differential logic unit with duplicated functional outputs. The logic functions as well as their inverses are implemented within a single Logic Unit (LU) cell. The hardware overhead for the implementation of the proposed LU is lower than the hardware overhead required for standard LU implemented with standard CMOS logic style. This new implementation is attractive as fewer transistors are required to implement important logic functions. The proposed differential logic unit can perform 8 Boolean logical operations by using only 16 transistors.

Spice simulations using a 32nm technology was utilized to evaluate the performance of the proposed circuit.

Keywords: *differential logic unit, double pass transistor logic, CMOS technology.*

1. Introduction

Conventional static CMOS has been a technique of choice in most processor design [1]. Alternatively, static pass transistor circuits have also been suggested for low-power applications [2].

Indeed, designing high-speed low-power circuits with CMOS technology has been a major research problem for many years. Several logic families have been proposed and used to improve circuit performance beyond that of conventional static CMOS family.

In addition, due to technology scaling and the increasing number of transistors on chip, the performance of static CMOS circuits comes at substantial area/power dissipation costs that may be critical, especially for portable appliances. New logic families that address the power and performance challenges must be therefore, explored [3].

The *Pass-Transistor Logic (PTL)* is a better way to implement circuits designed for low power applications. The advantage is that one pass-transistor network (either PMOS or NMOS) is sufficient to implement the logic function, which results in smaller number of transistors and smaller input load.

There are two main pass-transistor circuit styles: those that use NMOS only pass-transistor circuits, like CPL [4], and those that use both NMOS and PMOS pass-transistors, like DPL [5] and DVL [6].

Recently, several researchers have attempted to use Complementary pass transistor logic (CPL) to realize static and high performance designs in different digital systems [4–7].

However, since only NMOS transistors are used in CPL gates, the voltage swing at the end of a pass transistor network has a swing from 0 to $V_{DD} - V_{TH}$; therefore PMOS transistors at the following static gates are not completely off resulting in static power dissipation.

This problem is usually solved by a PMOS level restorer transistor to pull up the node to V_{DD}. The level restorer adds hysteresis to the gate and degrades the performance. Also, the delay of pass transistor networks increases quadratically with the number of stages and as a result, some intermediate buffers should be used to make strong V_{DD} and ground. All these problems arise from the fact that NMOS transistors can not pass V_{DD} faithfully to the other side. The solution is using a complementary PMOS transistor in parallel with NMOS to generate a strong V_{DD} at the output [8]. This structure is double pass transistor logic (DPL).

DPL uses both PMOS and NMOS devices in the pass-transistor network to avoid non full swing problems [9].

Double pass-transistor logic is shown to improve circuit performance at reduced supply voltage. Its symmetrical arrangement and double-transmission characteristics improve the gate speed without increasing the input capacitance [5].

In this paper, we propose a differential logic unit implemented in CMOS double pass transistor logic. The proposed logic unit (LU) is low power and small number of transistors design. It performs 8 logic functions with only 16 transistors.

The paper is organized as follows. Section II describes the proposed design. In section III, we present the simulation results. Conclusions are given in section VI.

2. Proposed Design

ALU stands for the Arithmetic logic unit and it is an internal part of the processor which is used for all the mathematical and logical operations. The operations of the ALU include arithmetic operations such as addition, subtraction, multiplication and division of the binary values. It also, performs some logical operations such as AND, OR and XOR, integer arithmetic operations and Bit-shifting operations etc. ALU is the fundamental building block of the processor.

Today, modern computers contain very complex ALU for performing the complex calculations and logical operations inside the computer. The data or the operands are the input of the ALU and it generates the output as the result of the computation.

In some of the computers the ALU is divided into two units: Arithmetic unit and Logic unit.

Logic units are the building blocks of many important computational operations like arithmetic, multiplexer-demultiplexer, parity checker, sum generator, etc... Multifunctional logic operation is very much essential in this respect.

In this paper, a differential logic unit is proposed that can perform 8 Boolean logical operations by using only 16 transistors. The circuit is implemented using the double pass transistor logic (DPL).

The bit slice of the proposed differential logic unit performing XOR, XNOR OR, NOR, AND, NAND, V_{DD} and V_{SS} is given in Fig. 1. It performs: XOR/XNOR for $(SO,S1) = (0, 0)$, OR/NOR for $(SO,S1) = (0, 1)$, NAND/AND for $(SO,S1) = (1, 0)$ and V_{DD}/V_{SS} for $(SO,S1) = (1, 1)$.
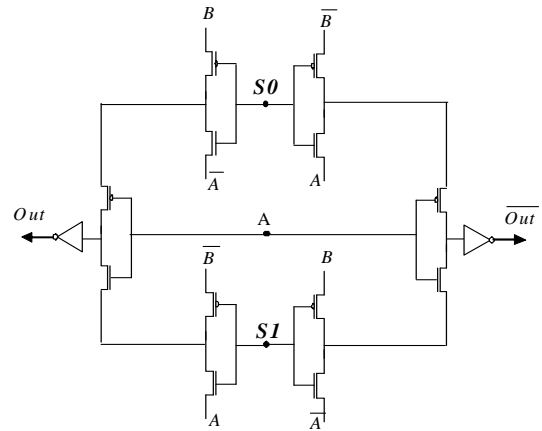

Fig. 1. The proposed differential logic unit

Fig. 1 shows a differential logic unit which consists of double pass transistors and inverter gates. Inputs A, S0 and S1 control the "ON" and "OFF" switching of the pass transistors.

Such obtained logic is differential as every variable is represented in its true and complement form.
Output inverters are added to ensure the drivability and outputs restoration.

The functions performed by the circuit of Fig. 1 are resumed in table I.

Table 1 : The Logic Unit truth table

Control		Logic operation	
SO	S1	Out	Outb
0	0	XOR	XNOR
0	1	OR	NOR
1	0	NAND	AND
1	1	0 (V_{SS})	1 (V_{DD})

The logic functions as well as their inverses are implemented within a single LU cell which is a multiplexer (Fig. 2).
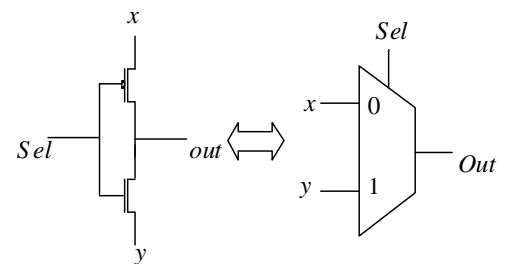

Fig. 2. The basic logic unit cell

A circuit that generates an output that exactly reflects state of one of a number of data inputs, based on value of one or more control inputs is called "multiplexer" [10].

Multiplexer is an important part in implementation of signal control systems and memory circuits, since it allows us to choose one of the inputs and transfer it to the output. The functionality of multiplexer is shown in (1). x and y are the two inputs and Sel is used to select one between the two inputs [11].

$$Out = x\,.Sel + y\,.\overline{Sel} \qquad (1)$$

The proposed logic unit is implemented using the double pass transistor logic. This structure uses only 16 transistors.

3. Simulation Results

Before implementing the whole circuit, a gate-level schematic in DSCH3 is generated. DSCH3 program is a logic editor and simulator used to validate the architecture of logical circuit, before microelectronics started. It provides user friendly environment for hierarchical logic design and fast simulation with delay analysis, which allows design and validation of complex logic structures.

After successful simulation we implemented the above designs of the logic unit with different components using Microwind 3.1 layout tool [12] for its ease of use and availability.

The differential logic unit of the Fig. 1 is implemented in full-custom 32nm CMOS technology at 0.8V power supply [12]. SPICE simulations of the circuit extracted from the layout, including parasitic, are used to demonstrate that this circuit has an acceptable electrical behavior. The layout of the differential logic unit with the two restoring inverters is as shown in Fig.3. It occupies an area of $0.93 \times 1.185 \mu m^2$.
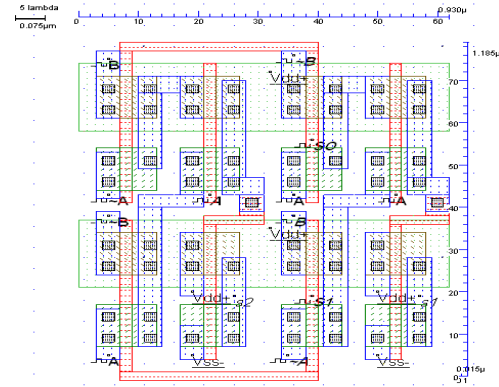

Fig. 3. Layout of the logic unit in CMOS 32nm Double Pass Transistor Logic

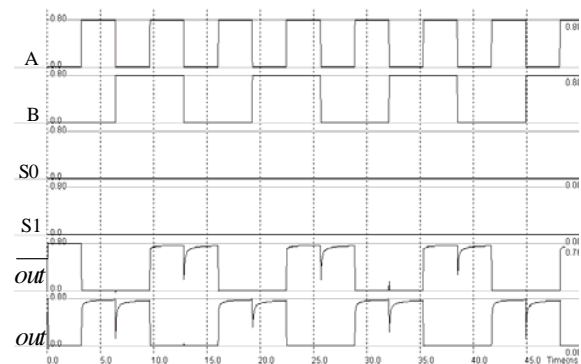Fig. 4, 5, 6 and 7 illustrates a SPICE simulation of the circuit of Fig. 3.

Fig. 4. The dual rail XOR/XNOR function for (S0, S1) = (0,0)

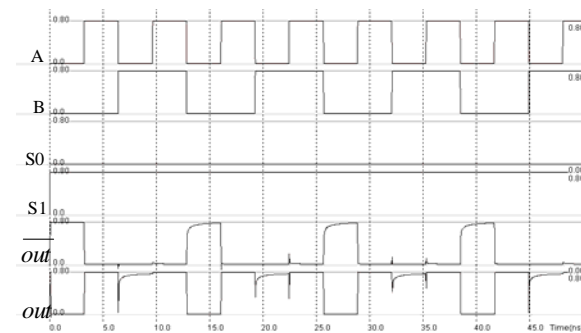The above simulation show that when (SO,S1) = (0,0), out = XOR and $\overline{out}$ = XNOR.

Fig. 5. The dual rail OR/NOR function for (S0, S1) = (0,1)

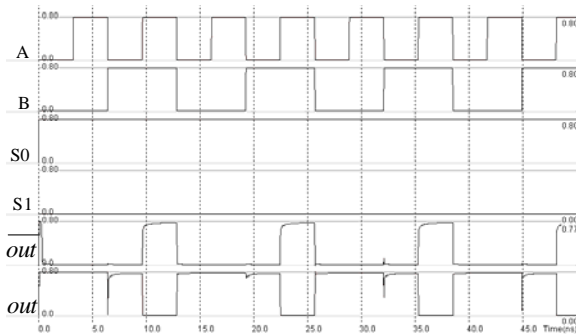When (SO,S1) = (0,1), out = OR and $\overline{out}$ = NOR.

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354

Fig. 6. The dual rail AND/NAND function for (S0, S1) = (1,0)

When (SO,S1) = (1,0), out = NAND and $\overline{out}$ = AND

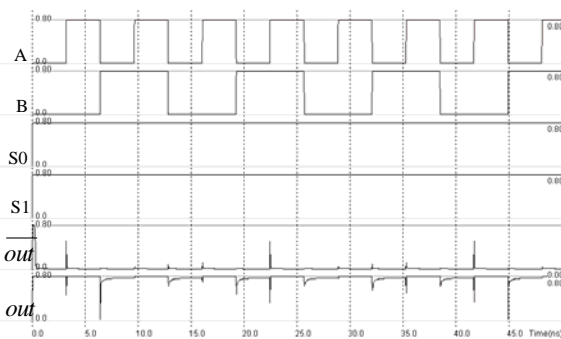

Fig. 7. The VDD/VSS function for (S0,S1) = (1,1)

For (SO,S1) = (1,1), out = V_{DD} and $\overline{out}$ = V_{SS}

Controlled by the two function select inputs (*S0* and *S1*), the logic unit can perform 8 possible logic operations using only 16 transistors.

The circuit is implemented with double pass transistor CMOS technology. Pass transistor logic is attractive as fewer transistors are needed to implement important logic functions, smaller transistors and smaller capacitances are required, and it is faster than conventional CMOS. However, the pass transistor gates generate degraded signals, which slow down signal propagation [13]. This degradation is corrected by inserting two inverters at the outputs of the circuit.

4. Conclusion

Logic units are the building blocks of many important computational operations like arithmetic, multiplexer-demultiplexer, parity checker, sum generator, etc...
In this paper, a new differential CMOS logic unit circuit based on double pass transistors is proposed. This implementation is low power, low cost design with only 16 transistors to perform 8 logic functions. In order to evaluate the usefulness of the proposed scheme, one bit Logic Unit was implemented and simulated. The proposed Logic Unit can operate at low voltages, yet giving quite a good speed.

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