Synthesis of Quantum Multiplexer Circuits

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Abstract

Combinational quantum circuits are essential for quantum computation; and quantum multiplexer circuit is one of the important combinational circuits. In this paper, we have presented the synthesis of quantum multiplexer circuit in detail. Instead of using functional blocks, we have used physically realizable quantum logic gates for synthesis of quantum multiplexers. In addition to this, our synthesis procedure shows that it is possible to construct quantum multiplexer circuit that can operate in the minimum dimension of the vector space and scalable according to linear nearest neighbor architecture. The detail functionality of the circuits along with the matrix formulations is presented.

Keywords: *Quantum Synthesis, Quantum Circuits, Quantum Multiplexer.*

Nomenclature

Qbit	Quantum bit
Qgate	Quantum gate
QNOT	Quantum NOT gate
LNN	Linear nearest neighbor
MUX	Multiplexer
CMUX	Classical digital multiplexer
QMUX	Quantum multiplexer
$\mathcal{H}_n$	n-dimensional Hilbert space, 2^n -dimensional vector space (n=1, 2, 3, … etc.)
CNOT	Quantum controlled-NOT gate with one control Qbit
C^nNOT	Quantum controlled-NOT gate with n number of control Qbits (n>1)
SWAP	Quantum swap gate
CSWAP	Quantum swap gate with one control Qbit
C^nSWAP	Quantum swap gate with n number of control Qbit (n>1)

1. Introduction

The pressure of fundamental limits on classical computation and the promise of exponential speedups from quantum mechanical effects are recently brought quantum circuits to a new dimensional attention of electronics community. As a result of which the quantum computation and information remain an attractive area of research in the last couple of decades. It is noticed that though wealth of knowledge in quantum mechanics is acquired; today development of quantum computer suffers from many aspects. Synthesis of quantum circuits is one of the major challenges in the quantum information processing and in the development of the architecture of quantum computer. Though some basic quantum logic circuits and gates are demonstrated, the efficient functional blocks such as quantum flip-flop, register, multiplexer, demultiplexer, counter etc. have not demonstrated and investigated rigorously to produce efficient quantum circuit which can be constructed by physically realizable Qgate. This paper deals with one of the combinational functional blocks such as QMUX which can be constructed by physically realizable gate such as CNOT gate.

In quantum computation, the Qbits are counterpart of the classical bits. Unlike bits which are described by two constants (0 and 1) and manipulated using Boolean algebra, Qbits are described in terms of vectors, matrices and manipulated using other linear algebra. The Qbits are realized in Hilbert space ($\mathcal{H}_1$) spanned by the orthogonal basis states $|0\rangle$ and $|1\rangle$, i.e.

$$\mathcal{H}_1 = \text{span}_{\mathbb{C}}\{|0>, |1>\} \quad (1)$$

A Qbit can be in a superposition state that combines $|0\rangle$ and $|1\rangle$. The states, $|0\rangle$ and $|1\rangle$ are the vectors of the computational basis and the value of a Qbit can be any unit vector in the space they span (i.e. in $\mathcal{H}_1$).

In addition to this, unlike the classical logic gate operation, the operation on Qbits must be reversible. The reversibility requirement of the operation on Qbits poses another challenge in the circuit synthesis. Both the logical and physical reversibility are the concern of any quantum circuits. If a circuit is logically reversible, then inputs can be constructed from the outputs of the circuit. For example, among the classical logic gates, NOT gate is the only reversible gate, but it is not a universal gate. While in quantum circuits, Fredkin gate, Toffoli gate (both having 3 inputs and 3 outputs) are the popular universal as well as reversible quantum gates. So in the cases, where the operation of a quantum circuit consists of many quantum operations, it is extremely important to check the reversibility of all the operations involved in that quantum circuit. Apart from these issues, Qbits cannot be copied using quantum wire in a similar way that we normally do

for classical circuits. Additionally, the number of inputs and outputs in any quantum circuit must be same.

The function of a MUX is to select one input among a group of inputs and pass the selected input to output of the circuit. Basically it consists of two types of inputs: one group is the data input and the other group is the select input and these select inputs decide which data input is to be selected to pass to the output. A classical "d:1 MUX" implies a MUX circuit with d number of data input and one output. A MUX circuit has numerous applications in information processing and communication.

Developing electronic functional block using another functional block is very common in electronics. For example, classical registers which are commonly composed of flip-flops. In such development, cost (of fabrication) and time taken for operation are mainly considered as efficiency of circuit. Recently, a few QMUX circuits are synthesized and presented [1,2].

The synthesis of QMUX using ternary quantum gates is also presented [2]. Since, the ternary quantum state is difficult to achieve and quite immature as a quantum effect, we have considered the most commonly used binary quantum state in the circuit synthesis procedure. Vivek et al. [3,4] and K. N. Patel et al. [5] presented many elements of the theory of quantum circuit to construct combinational circuits and we have extensively used their work in the synthesis of optimal QMUX.

In this work, we have shown that it is possible to develop QMUX circuit using physically realizable quantum logic gates. Open source software package 'Octave' is used as programming tool for this work. The operations involved in the proposed circuit are very basic in nature. We found that the number of operations and the cost of the proposed quantum circuit are optimum. The functionality of the circuit along with the reversibility requirement and matrix formulation are provided. The generalization of higher order QMUX synthesis is also presented.

2. Background

A combinational quantum logic circuit consists of quantum gates, interconnected by quantum wire carrying Qbits without fanout or feedback. Since, each quantum gate has the same number of inputs and outputs; any cut though the circuit crosses the same number of wires [3]. Quantum circuit operation is sequence of some quantum logic operations by some Qbits. A quantum wire is realized by a Qbit and corresponding matrix is a 2×2 identity matrix.

On the other hand, a quantum logic gate is a closed-system evolution (or transformation) of the n Qbit state space $\mathcal{H}_n$, i.e.

$\mathcal{H}_n = \text{span}_{\mathbb{C}}\{|q\rangle;\ q \text{ a bitstring of length } n\} = \text{span}_{\mathbb{C}}\{|q_1\rangle, |q_2\rangle, |q_3\rangle, |q_4\rangle \ldots\ldots\ldots\ldots\ldots |q_2{}^n\rangle\}$ (2a)

Where $|q_i\rangle = |b_0\ b_1\ b_2\ b_3\ b_4\ b_5 \ldots b_{n-1}\rangle = |b_0\rangle|b_1\rangle|b_2\rangle|b_3\rangle \ldots\ldots |b_n\rangle$ for each $b_i \in \{0,1\}$; $|b_0\ b_1\ b_2\ b_3\ b_4\ b_5 \ldots b_{n-1}\rangle$ is abbreviated as *bitstring state* and $|q\rangle = |\text{no of bits}\rangle$.

Here the arbitrary vector $|\psi\rangle$ ($|\psi\rangle \in \mathcal{H}_n$) can be written as

$|\psi\rangle = \alpha_1|000\ldots00\ldots000\rangle + \alpha_2|000\ldots00\ldots001\rangle + \alpha_3|000\ldots00\ldots010\rangle + \ldots\ldots\ldots + \alpha_i|000\ldots01\ldots101\rangle + \ldots\ldots\ldots + \alpha_n|111\ldots11\ldots111\rangle$ (2b)

$$|\psi\rangle = \sum_{q\in\mathbb{Q}^n} \alpha_i |q\rangle = \begin{pmatrix} \alpha_1 \\ \alpha_2 \\ \alpha_3 \\ \alpha_4 \\ . \\ . \\ \alpha_i \\ . \\ : \\ \alpha_{2^n} \end{pmatrix} \quad (2c)$$

Where, $\mathbb{Q}^n$ is the space of bitstring of length of n and $|\alpha_i|^2$ is the probability of the state of i^{th} element. So a n Qbit space is 2^n dimensional vector space and this can also be utilize as n Qbit register and a n Qbit circuit. Or in other words, no information is gained or lost during the transformation. Thus if $|q\rangle$ is a state vector in $\mathcal{H}_n$, the operation of n Qbit quantum logic gate can be represented by

$|q\rangle \rightarrow U|q\rangle$ (2d)

Where, U is the $2^n \times 2^n$ unitary matrix representing the gate operation.

Before we proceed to the synthesis of QMUX circuit, it is important to understand the effect of parallel and/or series combinations in quantum circuits and circuit elements used to construct the QMUX. We have used 2×2 SWAP gate and multiple controlled SWAP gate in the synthesis of QMUX. For the purpose of the quantum cost calculation, the multiple controlled SWAP gate is decomposed in terms of CNOT gate, controlled V gate and controlled $V^\dagger$. In the following paragraphs, we have presented these aspects of quantum circuits.

2.1 Combination of Quantum Circuit Elements

Combinational circuits are important to build a functional block. In order to demonstrate the effect of various combinations (series and parallel) of quantum gates and quantum wire in quantum circuits, a circuit shown in Fig. 1 is considered. The equivalent circuit is also shown in this figure.

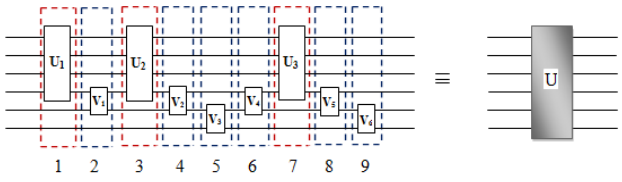


Fig. 1 A typical quantum logic circuits and its equivalence.

The circuit shown in Fig. 1 is a six Qbit quantum circuit and the circuit is composed of four Qbit and two Qbit quantum gates. The number of four and two Qbit Qgate in the circuit is 3 and 6 respectively. Note that the state of six Qbit circuit can be expressed by a vector in $\mathcal{H}_{6(n=6)}$ (contains 2^6 column element), whereas the four Qbit and two Qbit gates are expressed by unitary operations on $\mathcal{H}_{4(n=4)}$ and $\mathcal{H}_{2(n=2)}$. If U be the resultant unitary matrix representing the six Qbit circuit operation (the dimension of the U will be $2^6\times2^6$), then

$$U = \underset{1}{(I^{\otimes4}\otimes V_6)}\underset{2}{(I^{\otimes3}\otimes V_5\otimes I)}\underset{3}{(U_3\otimes I^{\otimes2})}\underset{4}{(I^{\otimes3}\otimes V_4\otimes I)}\underset{5}{(I^{\otimes4}\otimes V_3)}$$
$$\underset{6}{(I^{\otimes3}\otimes V_2\otimes I)}\underset{7}{(U_2\otimes I^{\otimes2})}\underset{8}{(I^{\otimes3}\otimes V_1\otimes I)}\underset{9}{(U_1\otimes I^{\otimes2})} \quad (3)$$

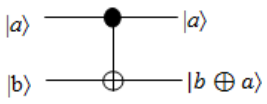
The number 1 to 9 at the top/bottom of the Equation (3) represents the individual operation of each block of circuit labeled by 1 to 9 in the circuit (see Fig. 1).

From the Equation (3) one can see that an individual operation can be represented by the tensor product (parallel combination of quantum wire and Qgate are represented by tensor product of corresponding unitary matrices of quantum circuit elements) of the corresponding space matrices while the linear combination of two individual operations is represented by the ordinary product of the individual space matrices. For example, consider the individual operation 1, which can be represented by the tensor product of U_1 and $I^{\otimes2}$ i.e. $(U_1\otimes I^{\otimes2})$. Similarly, the operation 2 can be represented by $(I^{\otimes3}\otimes V_1\otimes I)$, while series combination of the operations 1 and 2 is the multiplication of their space matrices i.e. $(I^{\otimes3}\otimes V_1\otimes I)(U_1\otimes I^{\otimes2})$.

Actually six Qbits go through the operation according to the quantum circuit to produce some output state. Ordinary products of nine consecutive operations are performed by the circuit to produce some output sates from the input states.

2.2 CNOT Gate

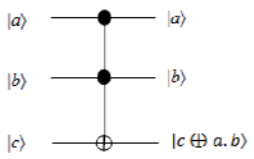
CNOT gate is one of the fundamental logic gates in quantum circuits and it operates in four (2^2) dimensional space. This gate consists of two inputs: one is the control input (a Qbit) and the other one is the target Qbit. The circuit and operational matrix U_{CNOT} ($2^2\times2^2$) of the CNOT gate is shown in Fig. 2. The operation of this gate can be written as $|\psi\rangle \rightarrow U_{CN}|\psi\rangle\rightarrow|a,b\oplus a\rangle$, where $|\psi\rangle=|a\rangle|b\rangle =|a\rangle\otimes|b\rangle$.



$$U_{CN} = \begin{pmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 \\ 0 & 0 & 1 & 0 \end{pmatrix}$$

Fig. 2 Circuit of CNOT gate and its matrix. Here $|a\rangle$ and $|b\rangle$ are the control and target Qbit respectively.

A three-input controlled-controlled-NOT gate in which two inputs act as control Qbit and the rest one acts as target Qbit is known as Toffoli gate (or C^2NOT gate) and is a universal quantum gate. This gate operates in 8 ($=2^3$) dimensional space. The circuit of the C^2NOT gate and its matrix U_T ($2^3\times2^3$) is shown in Fig. 3. The operation of this gate can be written as $|\psi\rangle \rightarrow U_T|\psi\rangle=U_T|a,b,c\rangle=|a,b,(c\oplus a.b)\rangle$.



$$U_T = \begin{pmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 \end{pmatrix}$$

Fig. 3 Circuit of C^2NOT gate (or Toffoli gate) along with its matrix. In this circuit $|a\rangle$, $|b\rangle$ are the two control Qbits and $|c\rangle$ is the target Qbit.

Though the CNOT gate is not directly involved in the synthesis of QMUX circuits, we have presented the above emphasis on CNOT gate since, we have used SWAP gate to construct QMUX circuits and SWAP gate consists of CNOT gate. In addition to this, CNOT gate is also involved in quantum cost calculation.

2.3 SWAP Gate

It swaps the states of two Qbits. The operation of this gate can be decomposed into three CNOT operations. The circuit for SWAP gate and its matrix U_S ($2^2\times2^2$) is shown in Fig. 4. The state ($|\psi\rangle=|a, b\rangle$) transformation for this gate can be represented as follows.

$|\psi\rangle \rightarrow U_S|\psi\rangle=U_S|a, b\rangle=|b, a\rangle$.

Or in other words,

$$|a,b\rangle \longrightarrow |a, a\oplus b\rangle$$
$$\longrightarrow |\, a\oplus (a\oplus b), a\oplus b\rangle = |b, a\oplus b\rangle$$
$$\longrightarrow |b, (a\oplus b)\oplus b\rangle = |b, a\rangle$$

Similar to CNOT gate, a SWAP gate can have also control Qbits. When the number of control Qbit is one, the gate

(CSWAP) becomes the well known Fredkin gate. The Fredkin gate is not only a reversible gate but also conservative, i.e. it is universal as well. Similar to Toffoli gate, the Fredkin gate also operates in space H_3. The swapping operation between the two target Qbits is performed when the control Qbit is $|1\rangle$ (active high) or $|0\rangle$ (active low). This means that the circuit can have two configurations: one is active high and other is the active low. The operational matrices (unitary matrices of dimension $2^3\times2^3$) of these two circuit configurations are different. The circuit configurations along with their unitary matrices for active high and active low are shown in Fig. 5 and Fig. 6 respectively.

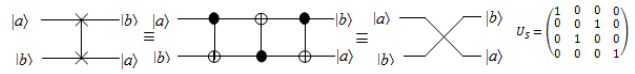


Fig. 4 Left to right: SWAP gate, equivalent circuit, equivalent symbol, SWAP gate matrix.

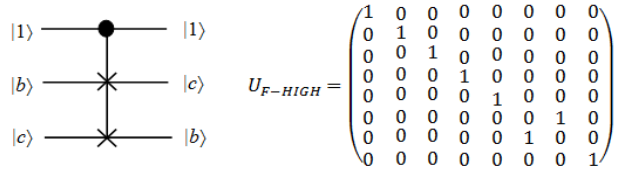


Fig. 5 Active high configuration of Fredkin gate and its matrix.

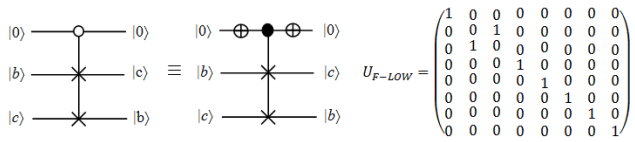


Fig. 6 Active low configuration of Fredkin gate, its equivalent circuit and its matrix.

Thus, when the number of control Qbit is increased to two, in a SWAP gate (i.e. for C^2SWAP gate), there exists four configurations for the swapping to be performed between the two target Qbits. The four circuit configurations along with their matrices are shown in Fig. 7.

3. Synthesis of QMUX

A CMUX consists of more than one input and only one output. The inputs of the multiplexer are two types: select inputs and data inputs. Depending upon the select inputs, at a time, only one of the data inputs is selected and sent to the output. If there are d data inputs in the circuit, then one needs at least s number of select input such that, $2^s \geq d$. This is the reason i.e. why commonly 2^n (where, n = 1, 2, ….etc.) number of data inputs are considered in the multiplexer circuit design. Unlike CMUX, the number of outputs of a QMUX is equal to the total number of inputs (which is valid to any quantum circuit) of the circuit. Among the (s+d) number of outputs, only one output shows the desired multiplexing property. For optimization we have designed the QMUX in such a way that the multiplexing output will be available at D_{o0}.

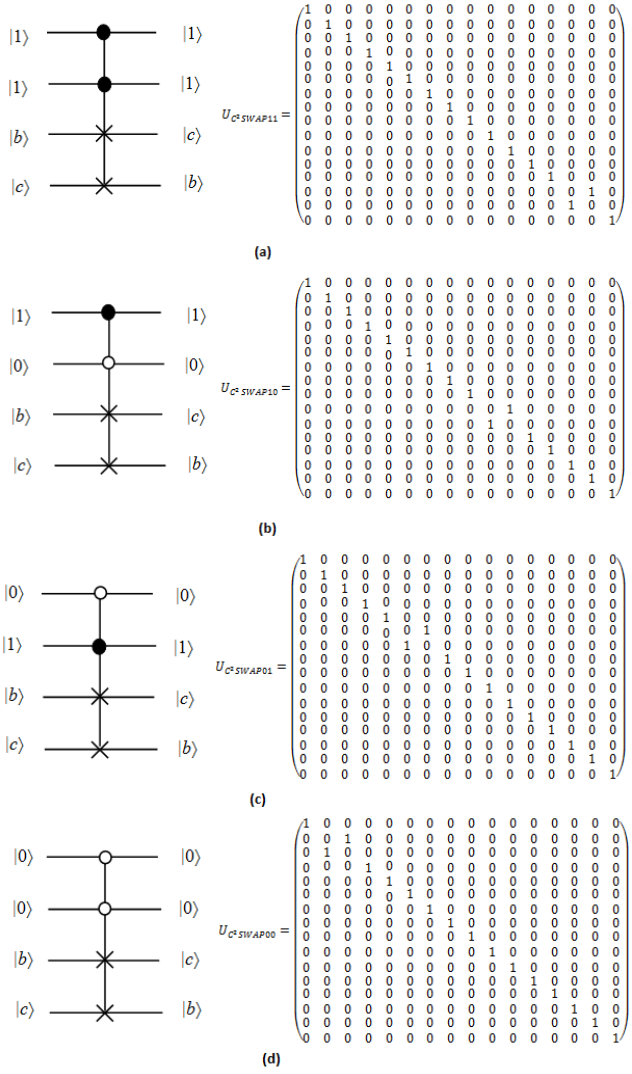


Fig. 7 Four configurations of the C^2SWAP gate and their matrices. Circuit swaps the target Qbits when both the control Qbits are set to $|1\rangle$, $|1\rangle$ for the configuration (a); $|1\rangle$, $|0\rangle$ for the configuration (b), $|0\rangle$, $|1\rangle$ for the configuration (c) and $|0\rangle$, $|0\rangle$ for the configuration (d).

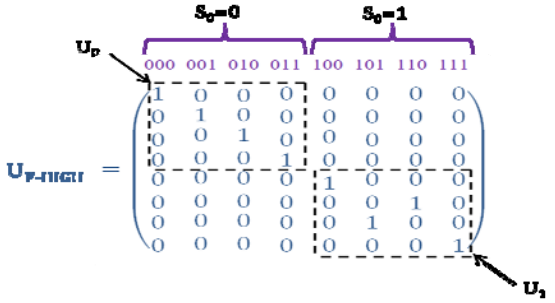
The matrix (M) of a QMUX is block diagonal [4]. If the QMUX consists of s and d number of select inputs and data Qbits respectively, then the matrix M will be a block diagonal matrix having 2^s blocks, each of size $2^d\times2^d$ [4]. Hence, the dimension of the matrix M will be $2^{d+s}\times2^{d+s}$. A typical matrix for QMUX is shown below.

$$U_{MUX} = \begin{pmatrix} U_0 & \cdots & \\ \vdots & \ddots & \vdots \\ & \cdots & U_{n-1} \end{pmatrix}$$; where, n – 1= 2^s.

3.1 Synthesis of 2:1 QMUX Circuit

The function of a 2:1 QMUX circuit can be performed by a Fredkin gate. A Fredkin gate can have two possible configurations (as shown earlier). Thus the possible two configurations along with their matrices of 2:1 QMUX can be found in Fig. 5 and Fig. 6. In these 2:1 QMUX circuits, the top most input Qbit is the control Qbit (or select input) and rest of two inputs are the data Qbits. Among the three output Qbits, the middle Qbit is the multiplexed Qbit. Let the states of the input Qbits for the circuit shown in Fig. 5 are: $|S_0\rangle$, $|D_{i0}\rangle$ and $|D_{i1}\rangle$ (from top to bottom) and the same for the output Qbits are: $|S_0\rangle$, $|D_{i0}\rangle$ and $|D_{i1}\rangle$ respectively, then we can express the state of the multiplexed output as: $|D_{i0}\rangle = |D_{i0} \oplus S_0 (D_{i1} \oplus S_0 D_{i0})\rangle$.

Let us consider the matrix $U_{F\text{-}HIGH}$ in Fig. 5 to explain its block diagonal nature. In this case, the number of select Qbit, s =1 and number of data input, d=2. Hence the number of the blocks in the said matrix is $2^s = 2$. The size of each block is $2^d \times 2^d = 4\times4$. To show the blocks of the matrix $U_{F\text{-}HIGH}$, it is rewritten as:



In the above expression, one can see the two blocks: U_0 and U_1 corresponds to the single select input $S_0 = 0$ or $S_0 = 1$. Note that the size of the each block is 4×4. In a more simplified way, the above matrix can be written as:

$$U_{F\text{-}HIGH} = \begin{pmatrix} U_0 & 0 \\ 0 & U_1 \end{pmatrix}$$

3.2 Synthesis of 4:1 QMUX Circuit

This circuit consists of 6 inputs among which 2 inputs are select inputs and 4 inputs are data inputs. The circuit of the 4:1 QMUX is shown in Fig. 8. The truth table of the circuit is shown in Table 1. In the truth table, each input Qbit is shown as 1 or 0 for simplicity, however in reality, each Qbit is a state vector either $|0\rangle$ or $|1\rangle$ (or superposition of these two sates) as shown earlier.

The dimension of the vector space ($\mathcal{H}_6$) which represents the 4:1 QMUX is 2^6. So for this circuit

$$\mathcal{H}_6 = span_{\mathbb{C}}(|b\rangle; b \text{ is bitstring of length } 6)$$
$$= span_{\mathbb{C}}(|b_1\rangle, |b_2\rangle \ldots |b_6\rangle)$$
$|b_i\rangle = |S_1 S_0 D_{i0} D_{i1} D_{i2} D_{i3}\rangle$;
Where, $S_1, S_0, D_{i0}, D_{i1}, D_{i2}, D_{i3} \in \{0,1\}$.

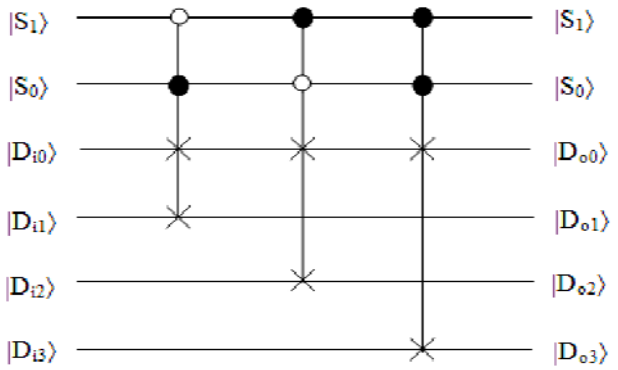


Fig. 8 Circuit of the 4:1 QMUX. Here, S_1, S_0 are two select input Qbits and D_{i3} to D_{i0} are the four data input Qbits. The quantum wire D_{o0} shows the multiplexing output.

Table 1: Truth table of 4:1 QMUX.

S_1	S_0	D_{i3}	D_{i2}	D_{i1}	D_{i0}	Output(D_{o0})
0	0	0	0	0	0	D_{i0}
0	0	0	0	0	0	D_{i0}
. . .	. . .	. . .	. . .	. . .	. . .	D_{i0}
0	0	1	1	1	1	D_{i0}
0	1	0	0	0	0	D_{i1}
0	1	0	0	0	1	D_{i1}
. . .	. . .	. . .	. . .	. . .	. . .	D_{i1}
0	1	1	1	1	1	D_{i1}
1	0	0	0	0	0	D_{i2}
1	0	0	0	0	1	D_{i2}
. . .	. . .	. . .	. . .	. . .	. . .	D_{i2}
1	0	1	1	1	1	D_{i2}
1	1	0	0	0	0	D_{i3}
1	1	0	0	0	1	D_{i3}
. . .	. . .	. . .	. . .	. . .	. . .	D_{i3}
1	1	1	1	1	1	D_{i3}

Now, if $|\Psi M\rangle$ is a state of the QMUX, then

$$|M\rangle \rightarrow \sum_{b\in\mathbb{B}^6} \alpha_i |b\rangle \rightarrow \begin{pmatrix} \alpha_1 \\ \alpha_2 \\ . \\ : \\ \alpha_{2^6} \end{pmatrix};$$

Where, $|\alpha_i|^2$ is the probability of the state of i^{th} element. So, a state of this space is basically realized by the above column vector. Similar to the previous multiplexer circuit, the matrix $U_{4:1\ QMUX}$ in the block diagonal form can be written as:

$$U_{4:1\ QMUX} = \begin{pmatrix} U_0 & & & \\ & U_1 & & \\ & & U_2 & \\ & & & U_3 \end{pmatrix}$$

Where U_0, U_1, U_2 and U_3 are the four diagonal blocks, each of size $2^4 \times 2^4$. So here U_0, U_1, U_2 and U_3 are operated on data inputs D_{i0}, D_{i1}, D_{i2} and D_{i3} when S_0=0, S_1=0; S_0=0, S_1=1; S_0=1, S_1=0; S_0=1, S_1=1 respectively.

In order to understand the operation of the QMUX in detail, the circuit is decomposed into nine functional blocks using LNN method. The LNN is often considered as an appropriate technique to scalable quantum architecture [6]. The decomposition of the circuit (using LNN method) is shown in Fig. 9.

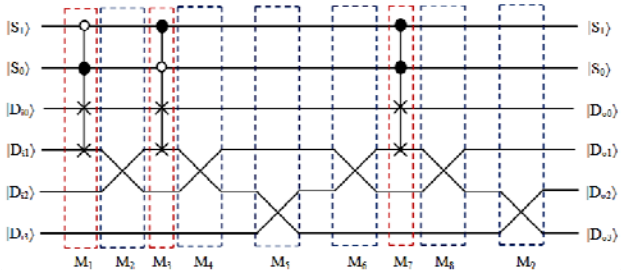


Fig. 9 Decomposition of 4:1 QMUX circuit into nine functional blocks.

Denoting I as 2×2 identity matrix, the matrices of the nine blocks are:

$M_1 = U_1 \otimes I^{\otimes 2}$ (where, $U_1 = U_C{}^2 swap_{01}$, see Fig. 7c)

$M_2 = I^{\otimes 3} \otimes U_S \otimes I$ (for U_S see Fig. 4)

$M_3 = U_2 \otimes I^{\otimes 2}$ (where, $U_2 = U_C{}^2 swap_{10}$, see Fig. 7b)

$M_4 = M_2$

$M_5 = I^{\otimes 4} \otimes U_S$

$M_6 = M_2$

$M_7 = U_3 \otimes I^{\otimes 2}$ (where, $U_3 = U_C{}^2 swap_{11}$, see Fig. 7a)

$M_8 = M_2$

$M_9 = M_5$

The operation of each block is represented by a $2^6 \times 2^6$ matrix. The resultant matrix $U_{4:1\ QMUX}$ of the 4:1 multiplexer circuit is, therefore the multiplication of the nine matrices, i.e.

$U_{4:1\ QMUX} = M_9 \times M_8 \times M_7 \times M_6 \times M_5 \times M_4 \times M_3 \times M_2 \times M_1$

The input and output of the 4:1 QMUX circuit is a column of matrix of element 64 ($2^{s+d} = 2^6 = 64$). If Γ represents an output matrix corresponding to the input matrix Λ of the circuit, then one can write, $U_{4:1\ QMUX}\ \Lambda = \Gamma$. This expression can also be written in the following form:

$$U_{4:1\ QMUX} \cdot \begin{pmatrix} \alpha_1 \\ \alpha_2 \\ \vdots \\ \alpha_r \\ \vdots \\ \alpha_{r+f} \\ \vdots \\ \alpha_{2^n} \end{pmatrix} = \begin{pmatrix} \alpha_1 \\ \alpha_2 \\ \vdots \\ \alpha_{r+f} \\ \vdots \\ \alpha_r \\ \vdots \\ \alpha_{2^n} \end{pmatrix} ; r \geq 17 \qquad (4)$$

In the Equation (4), n = s+d = 6 for 4:1 QMUX and the constraint, $r \geq (2^d + 1)$ or $r \geq 17$ is obtained as follows.

In Equation (4), the 17^{th} element is the square-root of the probability of the input state $|010000\rangle$. The 17^{th} position represents an element which changes its position according to combinations of select inputs other than all 0s. Here $|\alpha_r|^2$ stands for probability of r^{th} state which changes according to the circuit operations and swaps with $(r+f)^{th}$ state.

In order to check the reversibility of circuit, the unitary property of the matrix $U_{4:1\ QMUX}$ is checked. It is found that the relation: $(U_{4:1\ QMUX}).(U_{4:1\ QMUX})^T = I$ is valid for the circuit and hence the proposed multiplexer circuit is a reversible circuit.

3.3 Higher Order QMUX Synthesis

Considering the 4:1 QMUX circuit as reference, it is not difficult to construct a higher order multiplexer. By looking the sequences of 'O' and '●' and '×' in Fig. 8, one can easily construct an 11-input 8:1 QMUX circuit. Such an 8:1 QMUX circuit is shown in Fig. 10.

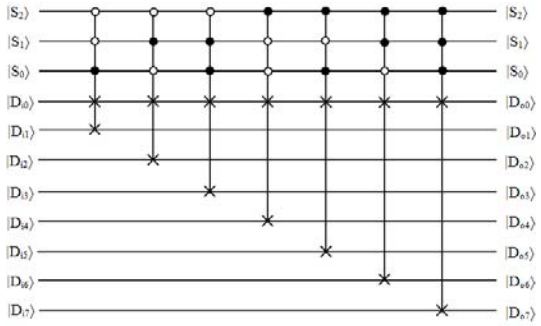


Fig. 10 An 11-input optimized 8:1 QMUX circuit.

Hence, it is possible to generalize the QMUX circuit for an n:1 QMUX, where $n = 2^r$, r is the number of select inputs. Such an optimistic generalized circuit is shown in Fig. 11.

4. Quantum Cost

Quantum cost is a measure of efficiency of a quantum circuit and it is commonly expressed in terms of Qgate. Using the LNN method, the quantum cost of different quantum gates is given in Table 2 [7].

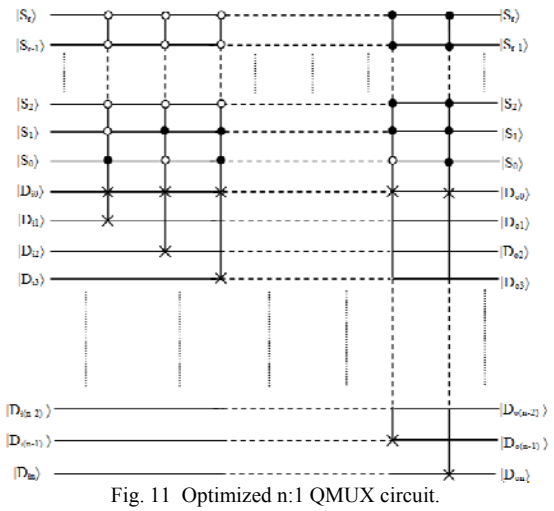


Fig. 11 Optimized n:1 QMUX circuit.

Table 2: Quantum cost of different Qgate [7].

Name of the Gate	Quantum cost
Controlled NOT	1
Controlled V	1
2-input SWAP	3
3-input Toffoli	9
4-input Toffoli	27
5-input Toffoli	45
3-input Fredkin	11
4-input Fredkin	29
5-input Fredkin	47

Similar technique is used to calculate the quantum cost for QMUX circuits and the summary of the cost calculation is presented in Table 3.

Table 3: Quantum cost for the QMUX circuits.

Order of Mux	No. of Select /contol inputs(S)	No. of Control swap Gates(G)	Total No. of input lines (T)	No. of SWAP Gates according to each block (No. of blocks B=(n-1))										Total No. swap of Gates	Total No. of Gates ($G+T_{swap}$)	Quantum Cost of QMUX
				B_1	B_2	B_3	B_4	B_5	B_6	B_7	B_8	…	B_{n-1}			
2:1	1	1	3	0								…		0	1	11
4:1	2	3	6	0	2	4						…		6	9	109
8:1	3	7	11	0	2	4	6	8	10	12		…		42	49	473
…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…	…
n:1	$\frac{\ln(n)}{\ln 2}$	n-1	S+G+1	B_{N1}	B_{N2}	B_{N3}	B_{N4}	B_{N5}	B_{N6}	B_{N7}	B_{N8}	…	$B_{N[n-1]}$	T_{nswap}	$G^2=(n-1)^2$	X

Where,

$B_{N1} = 0$

$B_{N2} = 2 \times 1$; $B_{N3} = 2 \times 2$;….; $B_{N(n-1)} = 2 \times (n-2)$

$T_{nswap} = [(n-2) \times (2 + B_{N(n-1)})]/2 \Rightarrow T_{nswap} = G^2 - G$

Cost $X = 2S\left(2^{(S-1)} - 1\right) + (18S - 7)(2^S - 1) + 3 \times T_{nswap} = R + (18S - 7)(2^S - 1) + 3 \times T_{nswap}$

Where, $R = 2S(2^{(S-1)} - 1)$ is the no. of QNOT gates required for a C^nSWAP gate.

5. Conclusion

We have synthesized optimum QMUX circuit. In order to construct the quantum multiplexer, some physically realizable quantum gates are used and 'Octave' programming tool is used to present the functionality of the circuits. The matrix formulations and operational behavior of the circuits are presented in details. Our procedure shows the ability to construct a general n:1 QMUX.

References

[1] D. Mukhopadhyay and A. Si, "Quantum multiplexer design and optimization applying genetic algorithm" International Journal of Computer Science Issues, Vol. 7, Issues 5, 2010, pp. 360-366.

[2] Mozammel H. A. Khan, "Design of reversible/quantum ternary multiplexer and demultiplexer", Engineering Letters, Vol. 13:2, 2006, pp. EL_13_2_3.

[3] Vivek V. Shende, Aditya K. Prasad, Igor L. Markov and John P. Hayes, "Synthesis of reversible logic circuits", IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems, Vol. 22, No. 6, 2003, pp. 710-722.

[4] Vivek V. Shende, Stephen S. Bullock and Igor L. Markov, "Synthesis of quantum logic circuits", IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems, Vol. 25, No. 6, 2006, pp. 1000-1010.

[5] K. N. Patel, I. L. Markov and J. P. Hayes, "Optimal synthesis of linear reversible circuits", Quantum Information and Computation, Vol. 8, No. 3&4, 2008, pp. 0282-0294.

[6] B. Kane, "A silicon-based nuclear spin quantum computer". Nature, Vol. 393, 1998, pp. 133-137.

[7] Marek Perkowski, Martin Lukac, Dipal Shah, and Michitaka Kameyama; "Synthesis of quantum circuits in Linear Nearest Neighbor model using Positive Davio Lattices" Facta Uni. Ser. Elec. Energ., Vol. 24, No. 1, 2011, pp. 73-89.

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