

Comment on “Quantum Multiplexer Designing and Optimization applying Genetic Algorithm”

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Abstract

We have noticed that many fundamental laws and rules of quantum-circuit are violated in a work published in International Journal of Computer Science Issues [1]. The authors of this published work presented a quantum multiplexing circuit which is composed of half-adders, i.e. quantum multiplexing functionality is claimed to achieve by using few units of quantum half-adder. The authors performed ‘qubit copying’, ‘fanout’ etc. in the quantum circuit which are prohibited. Apart from these, two quantum circuits are claimed to be equivalent to each other though their operational matrices are not same. In this article, we have explained the mentioned violations in details.

Keywords: Quantum Circuit, Quantum Multiplexer, Quantum Bit Copying.

1. Comment – I

1.1 Section A

The 4:1 QMUX proposed in the ref. [1] is constructed using four quantum half-adder circuit. According to the authors of Ref. [1], the dotted blocks in the QMUX circuits shown in Fig. 3 and Fig. 2 (fourth QHA section and its equivalent circuit) of Ref. [1] are equivalent circuit of QHA [2]. But if we simplify the QHA using CNOT, Controlled-square-root of NOT gate (i.e. CV gate) and Controlled-square-root of NOT adjoint (i.e. CV[†] gate) then the resulted circuit does not matches with the dotted portion of the circuits in Ref. [1]. Additionally, the tensor like symbol ‘⊗’ used the quantum circuits in Ref. [1] provides no meaningful operation.

The fourth QHA section of the multiplexer circuit and its equivalent circuit are shown in Fig. 2 of Ref. [1] and these circuits are repeated for ease of explanation and shown in Fig. 1 of this article.

The authors of Ref. [1] claim that the bottom circuit of the circuit shown Fig. 1 (a) is equivalent of the top circuit of the same figure. However, we found that this is not true. Next, we have provided an explanation to proof that the said circuits are not equivalent.

Proof: Since, the authors used non-conventional circuit symbol, first we assume tensor like symbol represents

CNOT gate and Controlled-Controlled tensor like symbol represents a Toffoli gate. Based on these assumptions we have re-drawn the circuit which is shown in Fig. 1 (b). Note that the assumed circuit is not too an equivalent of QHA circuit. The authors used some two-qubit gates to represent a desired circuit. This combination of the primitive gates can be optimized and such an optimized circuit is shown in Fig. 2.

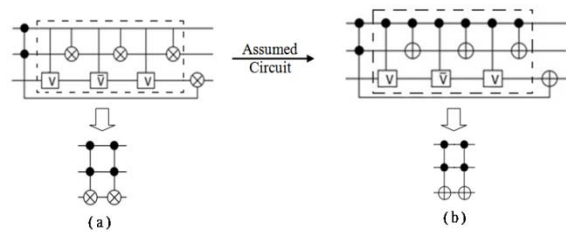


Fig. 1 (a) Fig. 2 of Ref. [1]. (b) Our assumed circuit of Fig. 1 (a).

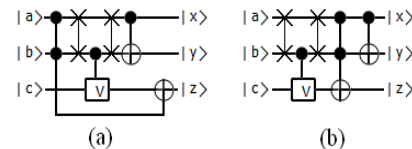


Fig. 2 (a) Optimized circuit of circuit shown in Fig. 1. (b) Equivalent of circuit of (a).

The equivalent circuit shown in Fig. 2(b) is obtained by applying moving rule and deletion rule [3] on the circuit shown in Fig. 2(a). The operational matrix of the circuit shown in Fig. 2 can be expressed as (with self explanatory notation):

$$M_1 = (U_{\text{SWAP}} \otimes \text{ID}) \cdot (\text{ID} \otimes U_V) \cdot (U_{\text{SWAP}} \otimes \text{ID}) \cdot U_{\text{Toffoli}} \cdot (U_{\text{CN}} \otimes \text{ID})$$

$$M_1 = \begin{pmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & \frac{1+i}{2} & \frac{1-i}{2} \\ 0 & 0 & 0 & 0 & 0 & 0 & \frac{1-i}{2} & \frac{1+i}{2} \\ 0 & 0 & 0 & 0 & \frac{1-i}{2} & \frac{1+i}{2} & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{1+i}{2} & \frac{1-i}{2} & 0 & 0 \end{pmatrix} \dots \text{Eq. (1)}$$

On the other hand, the operational matrix (M₂) of the

equivalent circuit shown in Fig. 1(b) (bottom circuit) can be expressed as:

$$M_2 = \begin{pmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 \end{pmatrix} \cdot \begin{pmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 \end{pmatrix} \dots \dots \dots \text{Eq(2)}$$

Since, the symbol used in the equivalent circuit (see Fig. 1(a)) is non conventional, we have assumed an equivalent circuit shown at the bottom of the Fig. 1(b) to derive the Eq. (2).

From Eq. (1) and (2), one can see that $M_1 \neq M_2$ and hence, the circuits are not equivalent to each other. Moreover, the matrix M_2 is an identity matrix, i.e. it represents quantum wire (since successive C^2 NOT operation gives the output same as input) in quantum circuit and it does nothing to the inputs. In short, the operational matrices of the circuits shown in Fig. 1 (top and bottom) are not identical and hence, they cannot be equivalent to each other.

1.2 Section B

Moreover, the authors claimed the dotted portion in the Fig 1(a) is an equivalent circuit of QHA, which is not true. The QHA circuit and its equivalent circuits are shown in Fig 3.

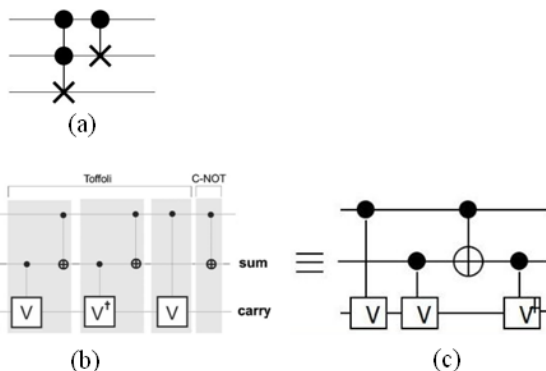
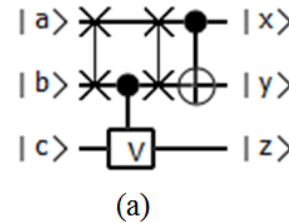


Fig. 3 (a) The QHA circuit. (b) and (c) are equivalent circuits of QHA.

The equivalent circuit of the dotted portion of the Fig. 1 (a) is shown in Fig. 4 (a). The operational matrix (M_3) of the dotted portion of the Fig 1(a) is computed and is shown in Fig. 4 (b). The operational matrix (M_4) of the QHA (circuit in Fig. 3) is shown in Fig. 4 (c). It is

therefore evident from the Fig. 4 that, $M_3 \neq M_4$. Hence, the dotted portion of the circuit does not represent a QHA which has been used in Ref. [1] to synthesize the multiplexer circuit.



$$M_3 = \begin{pmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & \frac{1+i}{2} & \frac{1-i}{2} \\ 0 & 0 & 0 & 0 & 0 & 0 & \frac{1-i}{2} & \frac{1+i}{2} \\ 0 & 0 & 0 & 0 & \frac{1+i}{2} & \frac{1-i}{2} & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{1-i}{2} & \frac{1+i}{2} & 0 & 0 \end{pmatrix}$$

(b)

$$M_4 = \begin{pmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 & 0 & 0 \end{pmatrix}$$

(c)

Fig. 4 (a) Equivalent circuit of dotted portion of Fig 1(a). (b) Its matrix. (c) Matrix of QHA.

2. Comment – II

In any quantum circuit; the number of input lines must equal to number the number of output lines along any cross-section of the circuit [4,5]. This rule is violated by the authors. For example, one can see the circuit shown in Fig. 3 of Ref. [1] (see page no. 365). In that circuit, the number of input line is seven while the number of output lines is nine. From this point of view, we can say that some copy operations exists in the circuit. Therefore, the proposed circuit is irreversible.

3. Comment – III

Copying (or Fanout) of qubit in quantum circuit is not allowed. This is because; copying of qubit from one quantum wire to another does not represent same state transformation to the copied quantum wire [5]. The transferred states could be different from the intended states. The authors violated this rule and some copy operations are considered into their circuits [1]. For example, one can see Fig. 3 on page 365 of the Ref. [1], in which many qubits are copied. In this circuit, the states like $|S_0\rangle$, $|S_1\rangle$ etc. are copied and shared among the circuit. The copying of qubit is shown by dotted arrow in Fig. 5.

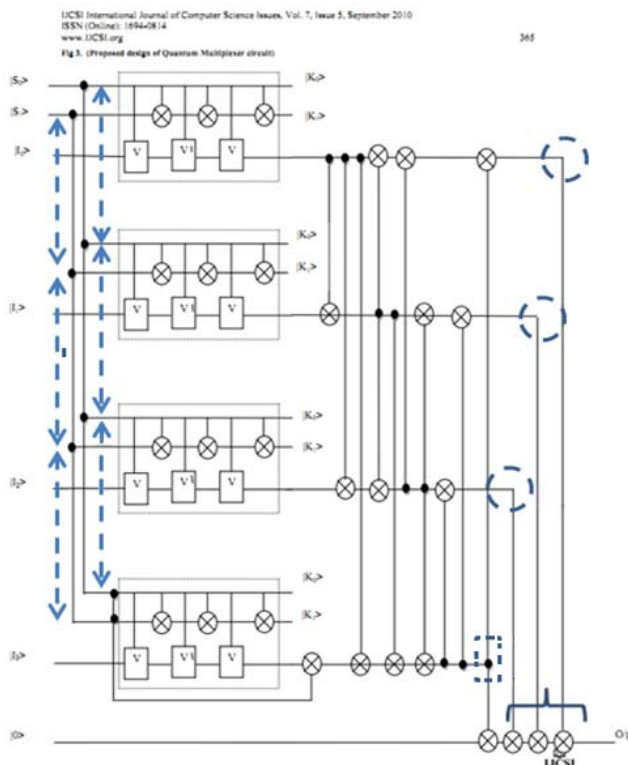


Fig. 5 A figure from Ref. 1 (page 365). The copying of qubits are shown by dotted arrows.

4. Comment – IV

The end of the line shown in Fig. 5 is prohibited in quantum circuit. In Ref. 1, the authors have represented a gate by '⊗' symbol. According to the description mentioned in Ref. 1, the gates shown by a brace in Fig. 5, are controlled gates for which '●' symbol should be used. However, no such symbol is used at position indicated by dotted circle in Fig. 5. Apart from these, the end of a line (shown by dotted circles and dotted square in Fig. 5) is presented in such a way which is possible in classical circuit but not in quantum circuit. Hence, four more output lines are hidden in this circuit and the actual number of

output lines raise to thirteen and number of input lines is seven, which in turn represents an irreversible quantum circuit and hence violating the law of quantum mechanics.

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