A Novel Architecture for Quantum-Dot Cellular Automata Multiplexer

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Abstract

Quantum-dot Cellular Automata (QCA) technology is attractive due to its low power consumption, fast speed and small dimension; therefore it is a promising alternative to CMOS technology. Additionally, multiplexer is a useful part in many important circuits. In this paper we propose a novel design of 2:1 MUX in QCA. Moreover, a 4:1 multiplexer, an XOR gate and a latch are proposed based on our 2:1 multiplexer design. The simulation results have been verified using the QCADesigner.

Keywords: *Quantum-Dot Cellular Automata (QCA), Nanotechnology, Circuit Design, Multiplexer, Circuit Simulation.*

1. Introduction

In VLSI technology, researchers face the physical limits of conventional CMOS technology. Due to this failure, they have switched to the novel nanotechnologies such as Single Electron Transistor (SET), Carbon nanotube (CNT) and Quantum-Dot Cellular Automata (QCA) [1]. QCA functions are based on Columbic interaction instead of current used in CMOS, so there is no leakage current. Additionally, it has major advantages such as low power consumption, high speed and small space consumption. QCA was presented in [2] for the first time and many circuits and designs have been introduced so far [3]-[5]. The basic structure in QCA is a cell that has four dots positioned at the corners of the squared cell and two free electrons. Each dot can be occupied by one of the two hopping electrons. Since the mutual behavior of the electrons is based on the Columbic interaction, they arrange themselves diagonally in order to reach to the maximum distance. Electrons can tunnel between dots through the barriers but cannot leave the cell; hence, there is no current flow. As shown in Figure 1 two stable polarization (p) states might occur, which represent the binary values “0” and “1”.

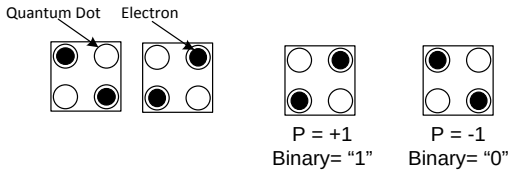


Fig. 1 QCA cell and the two stable polarizations.

The rest of this paper is organized as follows. Section 2 is dedicated to a brief review of previously introduced multiplexer designs. The proposed multiplexer is represented in section 2, as well. In section 3 we demonstrate simulation results and comparisons. Finally this paper is concluded in section 4.

2. QCA Review

In order to implement gates and circuits, QCA benefits from Columbic interaction between cells. An array of cells that are aligned can construct a QCA wire which is shown in Figure 2. The polarization of each cell in a QCA wire is directly affected by the polarization of its neighboring cells on account of electrostatic force. Accordingly, QCA wires can be used to propagate information from one end to another [6].

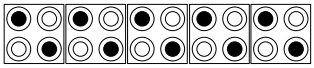


Fig. 2 QCA wire.

Two fundamental QCA gates are the inverter and the majority gate, (see Figure 3 and Figure 4). Many structures are implemented based on these two gates like the AOI [7], the complex gate [8] and one bit QCA full adder [9], [14] and [16].

2.1 Inverter Gate

Figure 3 shows three types of inverter gate; however, since the last one operates properly in all various circuits, it is used more in different designs compared to the two other types. This inverter is made of four QCA wires. The input polarization is split in-to two polarizations and in the end, two wires join and make the reverse polarization.

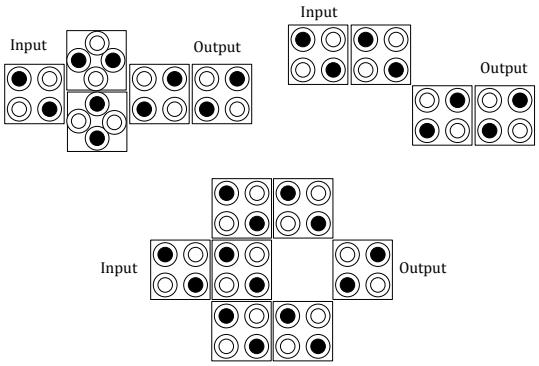
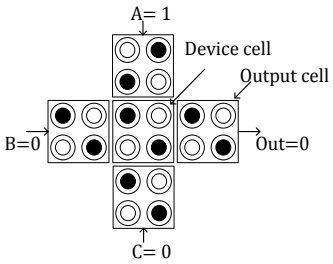


Fig. 3 Three types of inverter gate.

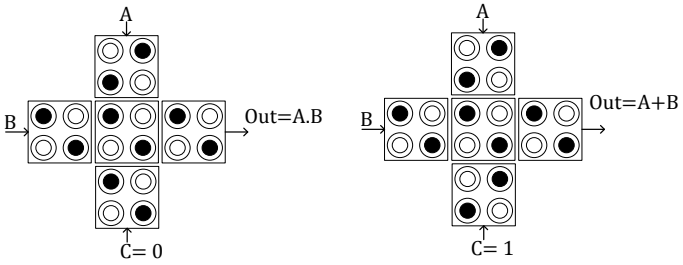
2.2 Majority Gate

Majority gate consists of five cells, three inputs, one output and a middle cell. The middle cell named device cell by reason of its function, switches to major polarization and determines the stable output. Majority gate can be programmed such that it functions as a 2-input AND or a 2-input OR by fixing one of the three input cells to p = -1 or p = +1, respectively. The Boolean expression of majority gate is as follows:

$$M(A,B,C) = AB + AC + BC \quad (1)$$



(a)



(b) (c)

Fig. 4 (a) The QCA majority gate. It can be programmed to function as (b) the AND gate or (c) the OR gate.

3. Multiplexer Design

Multiplexer is an important part in implementation of signal control systems and memory circuits, since it allows us to choose one of the inputs and transfer it to the output. The functionality of multiplexer is shown in (2). A and B are the two inputs and Sel is used to select one between the two inputs.

$$Out = A.Sel + B.\overline{Sel} \quad (2)$$

3.1 Previously Presented Multiplexers

Various formerly suggested implementations of a 2:1 multiplexer in QCA, have been studied and a novel efficient design is proposed. The proposed multiplexer is compared with the recent designs presented in [9]-[12] and [15] in terms of area, speed and complexity. Figure 5 shows the previously introduced multiplexer implementations. The Figure 5(a) depicts the multiplexer presented in [9]. As mentioned earlier, many QCA designs including multiplexer can be implemented based on majority gate. The equivalent expression based on majority function is as (3):

$$Out = Maj\left(Maj\left(In1, \overline{Sel}, 1\right), Maj\left(In1, Sel, 0\right), In0\right) \quad (3)$$

Two proposed multiplexers based on majority gate presented in [10], [11] are shown in Figure 5(b) and 5(c), respectively. Both of them are constructed in three layers, however, the latter is smaller and therefore more efficient.

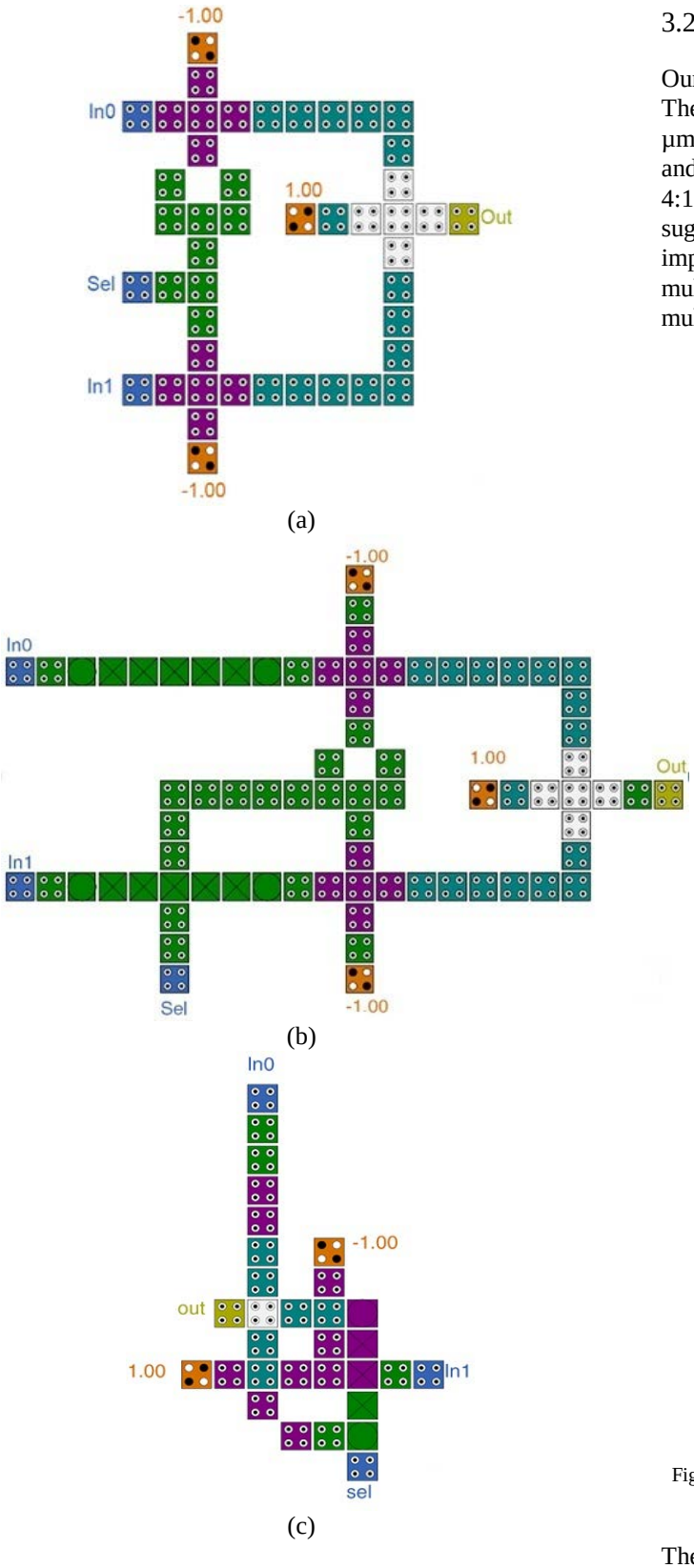


Fig. 5 Presented multiplexer (a) in [9], (b) in [10] and (c) in [11].

3.2 Proposed Multiplexer Design

Our 2:1 QCA multiplexer design is shown in Figure 6(a). The design consists of 27 cells covering an area of 0.03 μm^2. The proposed QCA multiplexer has been designed and simulated using the QCADesigner tool [12], [13]. A 4:1 multiplexer based on the proposed 2:1 multiplexer is suggested in Figure 6(b). This 4:1 multiplexer is implemented in two stages. We can construct larger multiplexers (8:1, 16:1 and so forth) using our 2:1 multiplexer design.

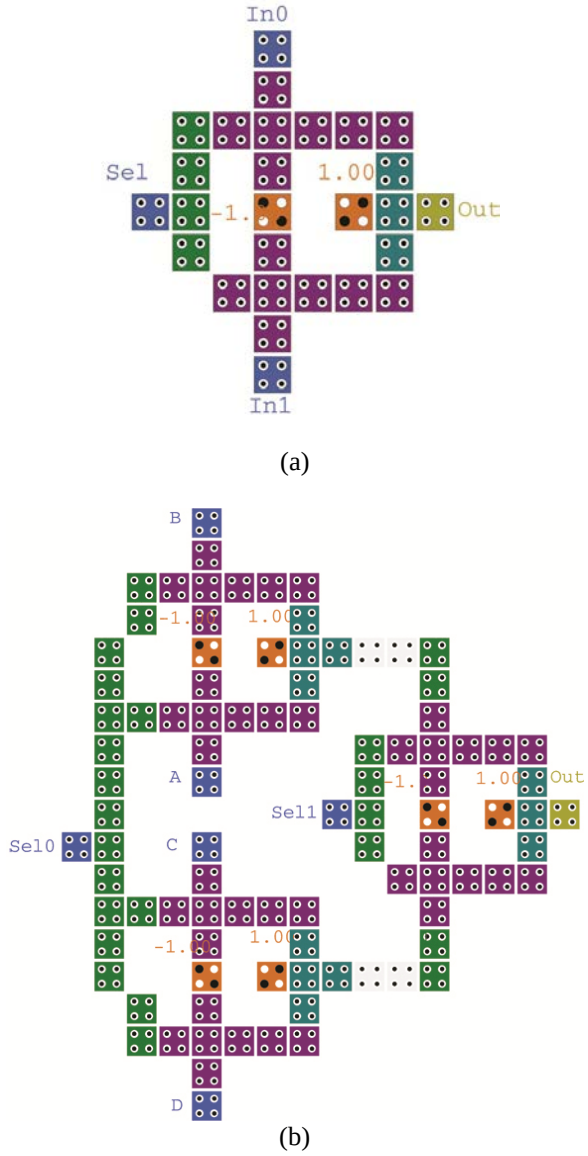


Fig. 6 (a) Schematic of proposed 2:1 multiplexer design, (b) Schematic of a 4:1 multiplexer.

The expression (4) is used for the 4:1 multiplexer. Its truth table is as Table 1.

$$Out = AS_1S_0 + BS_1\overline{S_0} + C\overline{S_1}S_0 + D\overline{S_1S_0} \quad (4)$$

Table 1: 4:1 Multiplexer truth table

S_1	S_0	Out
0	0	D
0	1	C
1	0	B
1	1	A

3.3 Sample Gates Based on Proposed Multiplexer

Different gates can be designed using our proposed 2:1 multiplexer. Two novel designs which are derived from the proposed multiplexer, are shown in Figure 7(a) and Figure 7(b). The former is an XOR and the latter is a latch.

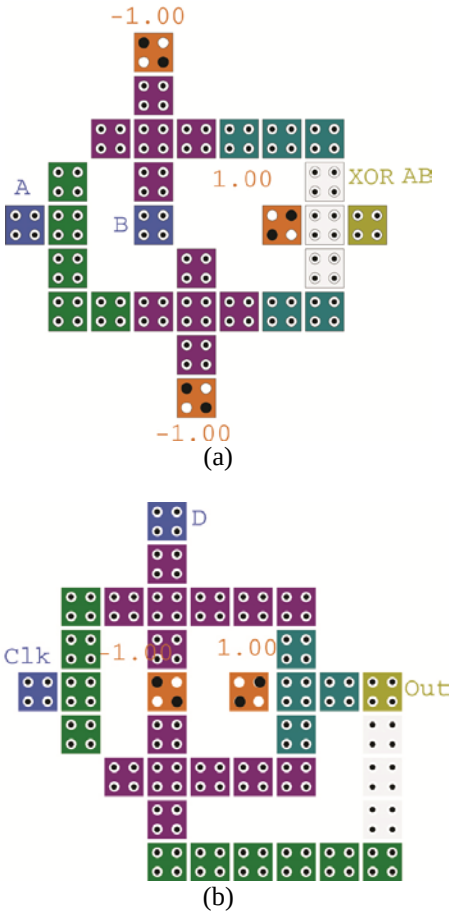


Fig. 7 (a) An XOR and (b) A latch based on proposed 2:1 multiplexer.

3.4 Simulation Result

The following parameters are used for a bistable approximation: cell size=18nm, number of samples=50000, convergence tolerance=0.0000100, radius of effect=65.000000nm, relative permittivity=12.900000, clock high=9.800000e–022 J, clock low=3.800000e–023 J, clock shift=0, clock amplitude factor=2.000000, layer separation=11.500000 and maximum iterations per sample=100. Most of the above mentioned parameters are default values in QCADesigner. Proposed 2:1 multiplexer and 4:1 multiplexer simulation results are provided with the input and output waveforms as shown in Figure 8.

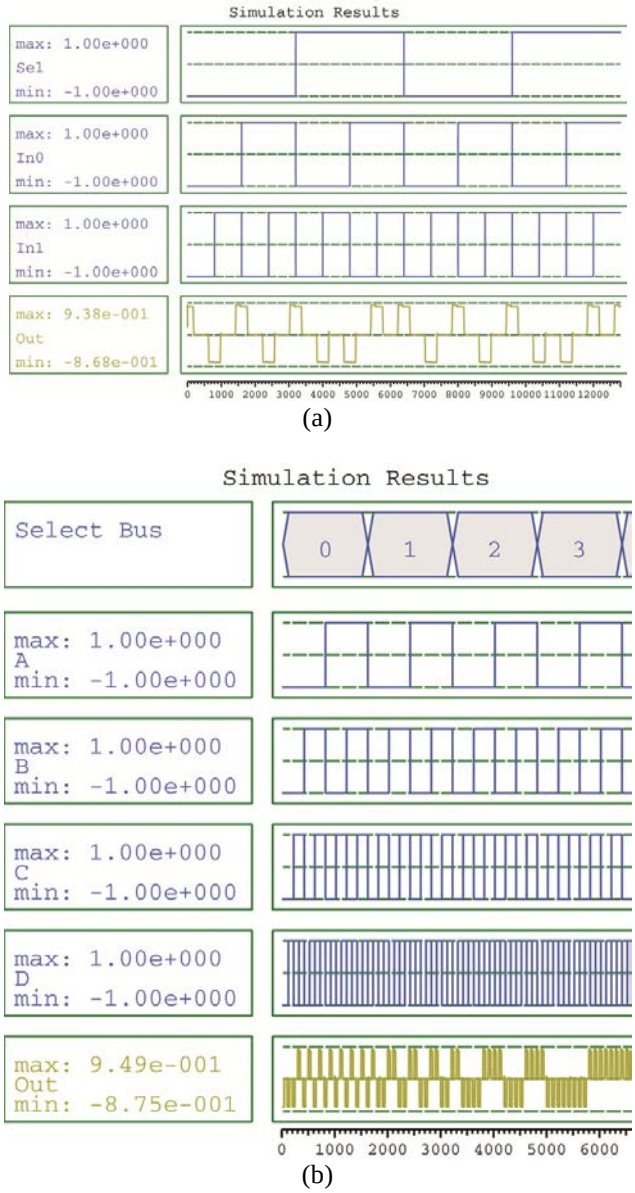


Fig. 8 (a) Simulation results of proposed 2:1 multiplexer, (b) Simulation result of 4:1 multiplexer based on proposed 2:1 multiplexer.

Figure 9 shows simulation results of an XOR gate and a latch.

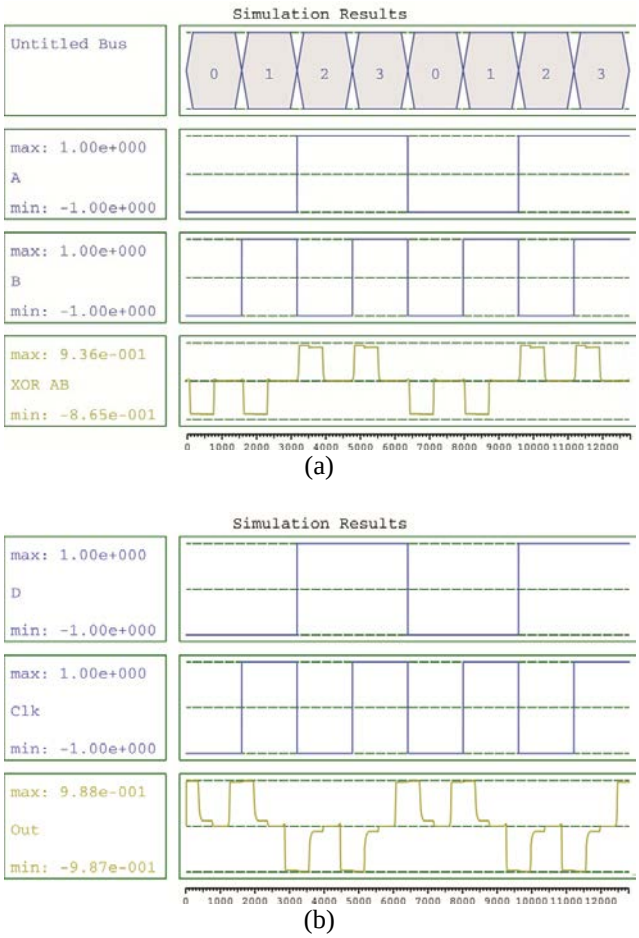


Fig. 9 Simulation results of (a) An XOR and (b) A latch based on 2:1 proposed multiplexer.

It is inferable from simulation results that the proposed multiplexer has achieved significant improvements in QCA circuits.

Table 2: Comparison of recent 2:1 multiplexer designs

2:1 Multiplexer	*Cell count*	*Area µm2*
Handmade presented in [9] Figure 6 (a)	88	0.14
Multiplexer presented in [10] Figure 6 (b)	46	0.08
Multiplexer presented in[11] Figure 6 (c)	36	0.06
Proposed Multiplexer Figure 7	27	0.03

4. Conclusion

Multiplexer is an important and fundamental element in most commonly used circuits. This paper presented a novel and efficient design of 2:1 QCA multiplexer. The proposed multiplexer gate and the other suggested gates which are structured by use of it, have been simulated using QCADesigner and tested in terms of complexity (cell count) and area. As it was apparent in simulation results, the proposed multiplexer has some superiority over the previous common designs in QCA and the comparisons evidently showed significant improvements.

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