Design of a High Performance Reversible Multiplier

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Abstract

Reversible logic circuits are increasingly used in power minimization having applications such as low power CMOS design, optical information processing, DNA computing, bioinformatics, quantum computing and nanotechnology. The problem of minimizing the number of garbage outputs is an important issue in reversible logic design. In this paper we propose a new 4×4 universal reversible logic gate. The proposed reversible gate can be used to synthesize any given Boolean functions. The proposed reversible gate also can be used as a full adder circuit. In this paper we have used Peres gate and the proposed Modified HNG (MHNG) gate to construct the reversible fault tolerant multiplier circuit. We show that the proposed 4×4 reversible multiplier circuit has lower hardware complexity and it is much better and optimized in terms of number of reversible gates and number of garbage outputs with compared to the existing counterparts.

Keywords: *Reversible logic circuit, reversible logic gates, reversible multiplier circuits, quantum computing, nanotechnology based systems.*

1. Introduction

Irreversible hardware computation results in power dissipation due to information loss. As demonstrated by R.Landauer in the early 1960s, irreversible hardware computation, regardless of its realization technique, results in energy dissipation due to the information loss[1]. According to his research, the combinational logic circuits dissipate heat in an order of $kT \ln 2$ joules of energy for every bit of information that is erased, where $k=1.3806505 \times 10^{-23}$ $m^2 kg^{-2} k^{-1}$ (joules Kelvin ^{1}) is the Boltzman constant and T is the operating temperature [1]. For room temperature T the amount of dissipating heat is small(i.e. 2.9×10^{-21} joule), but not negligible. The design that does not result in information loss is called reversible. It naturally takes care of heating generated due to the information loss. Such gates or circuits allow the reproduction of the inputs from observed outputs and we can determine the inputs from the outputs [3] [4] [5]. Thus reversibility will become an essential property in future circuit design. Reversible logic has applications in various research areas such as low power CMOS design, optical computing, quantum computing, bioinformatics, thermodynamic technology, DNA computing and nanotechnology.

The difference of reversible logic synthesis compared to binary logic synthesis can be summarized as follows[8]:

1) The gates used to implement the circuit have the equal number of inputs and outputs.
2) Every output of a gate, which is not used in the circuit, is a garbage signal. A good synthesis method minimizes the number of garbage signals.
3) The total number of constants at inputs of the gates is kept as low as possible.

4) A gate output can be used only once (the fanout count of each output is equal to one). If two copies of a signal are required, a copying circuit is used.
5) The resulting circuit is acyclic.

Any reversible gate performs the permutation of its input patterns only and realizes the functions that are reversible. If a reversible gate has *k* inputs, and therefore *k* outputs, then we call it a k×k reversible gate. Any reversible circuit design includes only the gates that are reversible.A reversible circuit should have the following features [4]:

1) Use minimum number of reversible logic gates.
2) Use minimum number of garbage outputs.
3) Use minimum constant inputs.

Every output of a gate, which is not used for further computations , is a garbage signal[8].The input that is added to an nxk function to make it reversible is called constant input [12]. In many computational units multiplication is a heavily used arithmetic operation. For the processors to have high speed multipliers is very important. In this paper, we present a reversible multiplier circuit using reversible MHNG gate. We demonstrate that the proposed reversible multiplier circuit is better than the existing counterparts in terms of number of gates, number of garbage outputs, number of constant inputs and hardware complexity [20] [21] [22] [23] [24].

2. Reversible Logic

The *n*-input *k*-output Boolean function f (x_1, x_2,…., x_n) (referred to as (n, k) function) is called reversible if:

1) The number of outputs is equal to the number of inputs;
2) Each input pattern maps to a unique output pattern[13].

In other words, reversible functions are those that perform permutations of the set of input vectors.

3. Reversible Logic Gates

An nxn reversible logic gate can be represented as:

$$I_V = (I_1, I_2, I_2,\ldots,I_N)$$

$$O_V = (O_1, O_2, O_3,\ldots,O_N)$$

Where I_v and O_v are input and output vectors respectively. Several reversible logic gates have been proposed in the past few decades. Some of them are: Feynman gate, FG [6], Toffoli gate, TG [7], Fredkin gate, FRG[15], Peres gate, PG [11], New Gate, NG [14], TSG gate, TSG [5], MKG gate, MKG [16] and HNG gate, HNG [18]. In this section we review these reversible logic gates. Some of them are presented to allow for comparison with existing studies.

3.1 Feynman gate (FG)

Feynman gate (FG), also known as controlled-not gate (1-CNOT), is a 2×2 gate that can be described by the equations:

$$I_v = (A, B)$$
$$O_v = (P = B, Q = A \oplus B)$$

where 'A' is control bit and 'B' is the data bit. It is shown in Fig. 1.

3.2 Fredkin gate (FRG)

Fredkin gate (FRG), also known as controlled permutation gate, is a 3x3 reversible logic gate. It can be represented as:

$$I_v = (A, B, C)$$
$$O_v = (P = A, Q = A'B \oplus AC, R = A'C \oplus AB)$$

Where I_v and O_v are input and output vectors. It is shown in Fig. 2. Fredkin Gate is a conservative gate, that is, the Hamming weight of its input vector is the same as the Hamming weight of its output vector.

3.3 Toffoli gate (TG)

Toffoli gate (TG), also known as controlled controlled-not (CCNOT), is a 3x3 reversible logic gate. The Toffoli gate can be represented as:

$$I_v = (A, B, C)$$
$$O_v = (P = A, Q = B, R = AB \oplus C)$$

Where I_v and O_v are input and output vectors. The Toffoli gate is shown in Fig. 3.

3.4 Peres gate (PG)

Peres gate (PG), also known as New Toffoli Gate(NTG), combining Toffoli gate and Feynman gate is a 3x3 reversible logic gate. It can be represented as:

$$I_v = (A, B, C)$$
$$O_v = (P = A, Q = A \oplus B, R = AB \oplus C)$$

Where I_v and O_v are the input and output vectors. The Peres gate is shown in Fig. 4. Peres gate is equal with the transformation produced by a Toffoli Gate followed by a Feynman Gate.

3.5 New gate (NG)

New gate (NG), is a 3x3 reversible gate. It can be represented as:

$$I_v = (A, B, C)$$
$$O_v = (P = A, Q = AB \oplus C, R = A'C' \oplus B')$$

Where I_v and O_v are the input and output vectors. The New gate is shown in Fig. 5.

3.6 TSG gate

TSG gate is a 4×4 reversible gate. The TSG gate is shown in Fig. 6., where each output is annotated with the corresponding logic expression:

$$I_v = (A, B, C, D)$$
$$O_v = (P = A, Q = A'C' \oplus B, R = (A'C' \oplus B') \oplus D,$$
$$S = (A'C' \oplus B') D \oplus (AB \oplus C))$$

3.7 MKG gate

MKG gate is a 4x4 reversible logic gate. The MKG gate can be represented as:

$$I_v = (A, B, C, D)$$
$$O_v = (P = A, Q = C, R = (A'D' \oplus B') \oplus C,$$
$$S = (A'D' \oplus B').C \oplus (AB \oplus D))$$

Where I_v and O_v are the input and output vectors. The MKG gate is shown in Fig. 7., where each output is annotated with the corresponding logic expression.

3.8 HNG gate

The HNG gate is universal. The HNG gate is shown in Fig.8., where each output is annotated with the corresponding logic expression. The corresponding logic expression of HNG gate:

$$I_v = (A, B, C, D)$$
$$O_v = (P = A, Q = B, R = A \oplus B \oplus C,$$
$$S = (A \oplus B).C \oplus AB \oplus D)$$

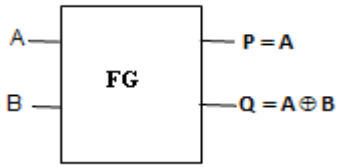

Fig. 1 Feynman Gate

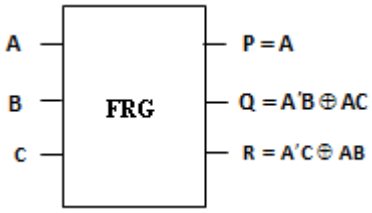

Fig. 2 Fredking gate

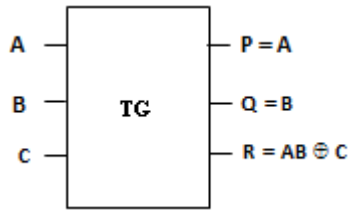

Fig. 3 Toffoli Gate

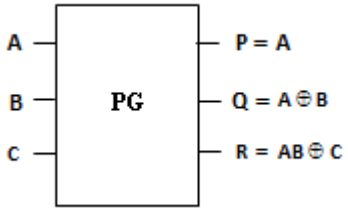

Fig. 4 Peres Gate

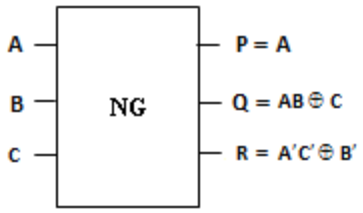

Fig. 5 New Gate

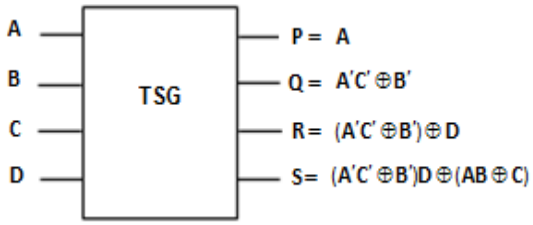

Fig. 6 TSG Gate

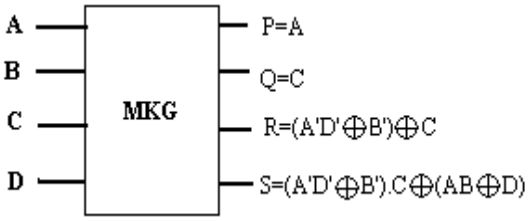

Fig. 7 Reversible MKG Gate

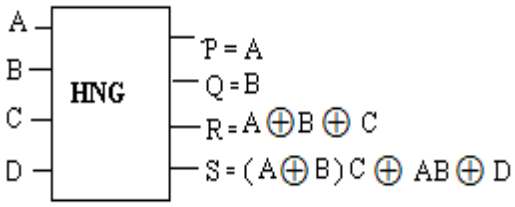

Fig. 8 Reversible HNG Gate

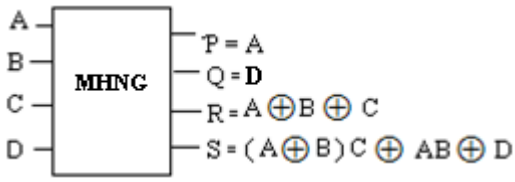

Fig. 9 Reversible MHNG Gate

4. Proposed Modified HNG Gate

Our proposed Modified HNG (MHNG) gate is a 4×4 reversible logic gate. The corresponding logic expression of MHNG gate:

$$I_v = (A, B, C, D)$$
$$O_v = (P = A, Q = D, R = A \oplus B \oplus C,$$
$$S = (A \oplus B).C \oplus AB \oplus D)$$

Where, I_v and O_v are the input and output vectors. The MHNG gate is shown in Fig .9, where each output is annotated with the corresponding logic expression.

The corresponding truth table of the MHNG gate is depicted in Table 1.

Table 1: Truth Table for Proposed Reversible MHNG gate

A	*B*	*C*	*D*	*P*	*Q*	*R*	*S*
0	0	0	0	0	0	0	0
0	0	0	1	0	1	0	1
0	0	1	0	0	0	1	0
0	0	1	1	0	1	1	1
0	1	0	0	0	0	1	0
0	1	0	1	0	1	1	1
0	1	1	0	0	0	0	1
0	1	1	1	0	1	0	0
1	0	0	0	1	0	1	0
1	0	0	1	1	1	1	1
1	0	1	0	1	0	0	1
1	0	1	1	1	1	0	0
1	1	0	0	1	0	0	1
1	1	0	1	1	1	0	0
1	1	1	0	1	0	1	1
1	1	1	1	1	1	1	0

One of the prominent functionalities of the MHNG gate is that it can work singly as a reversible full adder unit. If I_v = (A, B, C_{in}, 0), then the output vector becomes: O_v=(P=A, Q=0, R=Sum, S=C_{out}). Therefore, we have both of the required outputs. Implementation of the MHNG gate as the reversible full adder is shown in Fig. 10. The proposed reversible full adder circuit uses only one reversible logic gate. It produces only two garbage outputs. It requires only one constant input.

Let,

a = A two input EX-OR gate calculation
ß = A two input AND gate calculation

d = A NOT calculation
T = Total logical calculation

For [5]: T=6a+3ß+3d, for [16]: T=5a+3ß+3d , for [18]: T=5a+2ß and for proposed MHNG gate : T=5a+2ß. Thus, the proposed reversible full adder is better than the reversible full adder circuits in [5,16,18] in term of hardware complexity.

MHNG gate also performs as reversible half adder . If I_v = (0, B, C_{in}, 0), then the output vector becomes: O_v=(P = 0, Q=0, R=Sum, S=C_{out}). Implementation of the MHNG gate as the reversible half adder is shown in Fig. 11.

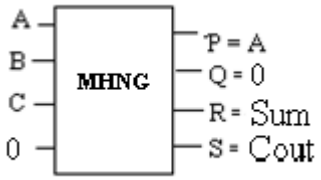

Fig. 10 MHNG Full Adder

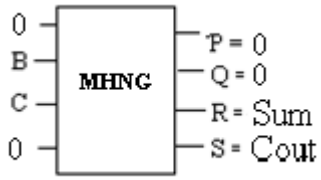

Fig. 11 MHNG half Adder

We will use MHNG gates to construct the novel reversible multiplier circuit.

5. Reversible Multiplier Circuit

The operation of the 4x4 multiplier is depicted in Fig. 12. It consists of 16 partial product bits of the form $x_i.y_i$. The proposed reversible 4x4 multiplier circuit has two parts. First, the partial products are generated in parallel using Toffoli and Peres gates [23]. Then, the addition is performed as shown in Fig. 13 .

The basic cell for such a multiplier is a full adder (FA) accepting three bits. We use MHNG gates as reversible full adder which is depicted in Fig. 10. The proposed reversible multiplier circuit uses eight reversible MHNG full adders. In addition, it needs four reversible half adders. It is possible to use MHNG gate as half adder, but we use Peres gate as reversible half adder because it has less hardware complexity compared to the MHNG gate.

6. Evaluation of Reversible Multiplier Circuit

The proposed reversible multiplier circuit is more efficient than the existing circuits presented in [19] [20] [21] [22] [23] [24]. Evaluation can be comprehended easily with the help of the comparative results in Table2. One of the main factors of a circuit is its hardware complexity. We can prove that our proposed circuits are better than the existing approaches in term of hardware complexity.

Let,
a = A two input EX-OR gate calculation
ß = A two input AND gate calculation
d = A NOT calculation
T = Total logical calculation

			x_3	x_2	x_1	x_0	
		x	y_3	y_2	y_1	y_0	
			x_3y_0	x_2y_0	x_1y_0	x_0y_0	
		x_3y_1	x_2y_1	x_1y_1	x_0y_1		
	x_3y_2	x_2y_2	x_1y_2	x_0y_2			
x_3y_3	x_2y_3	x_1y_3	x_0y_3				
P_7	P_6	P_5	P_4	P_3	P_2	P_1	P_0

Fig. 12 Partial products in a 4x4 multiplication

For [19] the Total logical calculation is:T=80a+100ß+68d, for [20] the Total logical calculation is: T=110a+103ß+71d, for [21] the Total logical calculation is: T=92a+52ß+36d ,for [22] the Total logical calculation is: T=80a+36ß, for [23] the Total logical calculation is: T=71a+36ß, for [24] the Total logical calculation is: T=71a+35ß, and for our proposed reversible multiplier circuit, the Total logical calculation is: T=80a+36ß. Therefore, the proposed reversible multiplier circuit is better than the existing circuits[19][20][21] in term of complexity.

Our proposed reversible 4×4 multiplier circuit is shown in Fig.13. We used eight reversible MHNG full adders and four reversible half adders.

In the proposed reversible multiplier circuit we use MHNG gate as reversible full adder and it produces

zero (0) in second output, which we have used as the fourth input for the next MHNG full adder circuit. Thus this proposed reversible 4×4 multiplier circuit produces less garbage outputs than the existing counterparts in [19]-[24].

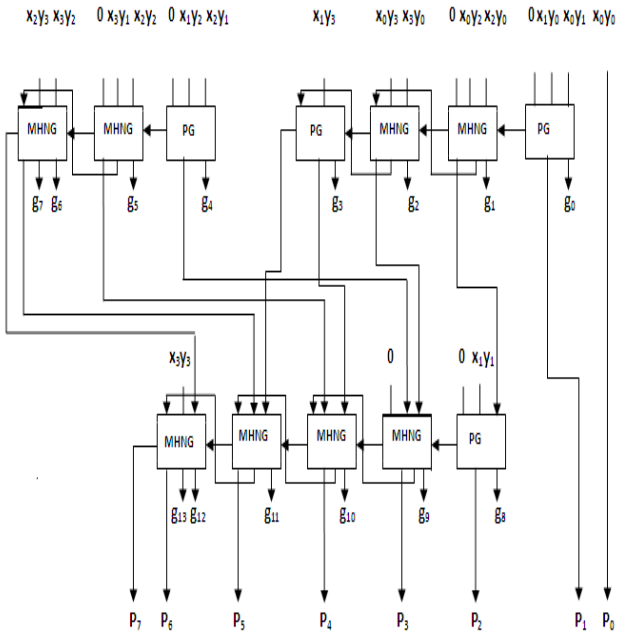

Fig. 13 Proposed 4x4 reversible multiplier circuit using MHNG gates and Peres gates.

Table 2: Comparative Experimental Results of Different Reversible Multiplier Circuits.

Paper No.	*No. of Gates*	*No. of Garbage Outputs*	*No. of Constant Inputs*	*Total Logical Calculation*
This Work	28	22	28	80a+36ß
[24]	28	32	28	71a+35ß
[23]	28	28	28	71a+36ß
[22]	28	52	28	80a+36ß
[21]	28	56	32	92a+52ß+36d
[20]	29	58	34	110a+103ß+71d
[19]	40	56	31	80a+100ß+68d

7.Results and Discussion

The proposed reversible multiplier circuit is more efficient then the existing circuit presented in [19] – [24]. Evaluation of proposed circuit can be comprehended easily with the help of the comparative results in Table 2. The difference between partial products generation design with the existing designs in [19, 20, 21, 22, 24] is the use of Toffoli gates and Peres gates. This structure is proposed in [23]. This design method of generating partial product has less hardware complexity. Therefore, the proposed reversible multiplier circuit is better than the existing circuits in terms of complexity.

One of the other major constrains in designing a reversible logic circuit is less number of garbage output, but the design in [19] produces 56 garbage outputs, the design in [20] produces 58 garbage outputs, the design in [21] produces 56 garbage outputs, the design in [22] produces 52 garbage outputs, the design in [23] produces 28 garbage outputs, the design in [24] produces 32 garbage So, we can state that our design approach is better than all the existing counterparts in term of number of garbage outputs.

Number of constant inputs is one of the other main factors in designing a reversible logic circuit. Our proposed reversible multiplier circuit requires 28 constant inputs, but the [19] requires 31 constant inputs, the design in [20] requires 34 constant inputs, the design in [21] requires 32 constant inputs , the design in [22] requires 28 constant inputs, the design in [23] requires 28 constant inputs, the design in [23] requires 28 constant inputs So, we can state that our design approach is better than all the existing designs in term of number of constant inputs.

Comparing our proposed reversible multiplier circuit with the existing circuits in [19]- [24], it is found that the proposed design approach requires 28 reversible logic gates but the existing design in [19] requires 40 reversible gates, the existing design in [20] requires 29 reversible gates, the existing design in [21] requires 28 reversible gates, the existing design in [22] requires 28 reversible gates, the existing design in [23] requires 28 reversible g ates and the existing design in [24] requires 28 reversible gates. So, the proposed circuit is better than [19] [20] [21] [22][23][24] in term of number of reversible logic gates, which is one of the other main factors in reversible circuit design.

From the above discussion we can conclude that the proposed reversible multiplier circuit is better than all the existing design.

8. Conclusions

In this paper, we presented a 4x4 bit reversible multiplier circuit using MHNG gates, Toffoli gates and Peres gates. Table II demonstrates that the proposed reversible multiplier circuit is better than the existing designs in terms of hardware complexity, number of logic gates, garbage outputs, constant inputs and optimized in terms of area and delay time. Our proposed reversible multiplier circuit can be applied to the design of complex systems in nanotechnology.

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