Development of MIL-STD-1553B Synthesizable IP Core for Avionic Applications

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Abstract

MIL-STD-1553, Digital Time Division Command/Response Multiplex Data Bus, is a military standard (presently in revision B), which has become one of the basic tools being used today for integration of weapon systems. The standard describes the method of communication and the electrical interface requirements for subsystems connected to the data bus. The 1 Mbps serial communication bus is used to achieve aircraft avionic (MIL-STD-1553B) and stores management (MILSTD-1760B) integration. The standard defines four hardware elements. These are 1) The transmission media, 2) Remote terminals, 3) Bus controllers, 4) Bus monitors.

The main objective of this paper is to develop an IP (Intellectual Property) core for the MIL-STD-1553 IC. This IP core can be used as bus monitors or remote terminals or bus monitors. The main advantage of this IP core is to provide small foot print, flexibility and reduce the cost of the system, as we can integrate this with other logic.

1. Introduction

MIL-STD-1553B defines a serial, time division, multiplex command/response data bus. I.e. information is transferred by transmitting a series of data bits one after another; a single transmission path is shared between a number of users by the allocation of time to each user; all transactions take place in response to a command from a single controller. Bus topology is implemented using twisted pair transmission line terminated at each end in its characteristic impedance. Connections are made to the bus via stubs. The standard defines the characteristics of the bus cable, its termination and gives two alternative methods of connecting stubs to the bus 1) Direct coupled and 2) Transformer coupled.

The standard defines three types of terminals. They are bus controller, remote terminal and bus monitor. Bus controller has overall control of all bus activity. All transmissions over the bus are initiated by a command from the bus Controller

The number of remote terminals connected to the bus can be 31 in the range 0-30. Each remote terminal has a unique address. The remote terminals continuously monitor the bus and it receives the message which carries its address. These messages contain the actions to be performed by the remote terminal. The bus monitor monitors the bus and information obtained may be used for offline applications or as a backup. The standard provides the use of two bus for redundancy. The sample bus architecture is given in figure 1.

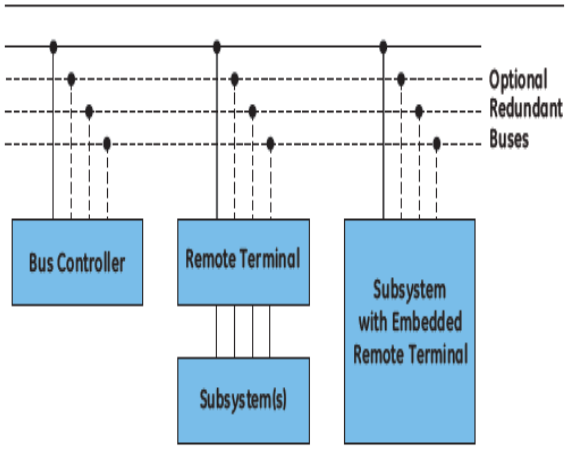

Fig 1:Sample data bus architecture.

The standard provides three types of words and ten types of word formats. Three types of words are:

a) Command word
b) Data word
c) Status word

Command word is issued by bus controller to the remote terminals. Data word can be transmitted by bus controller or remote terminals. The status word is transmitted by the remote terminal to the bus controller in response to the command word. Figure 2 shows different types of words.

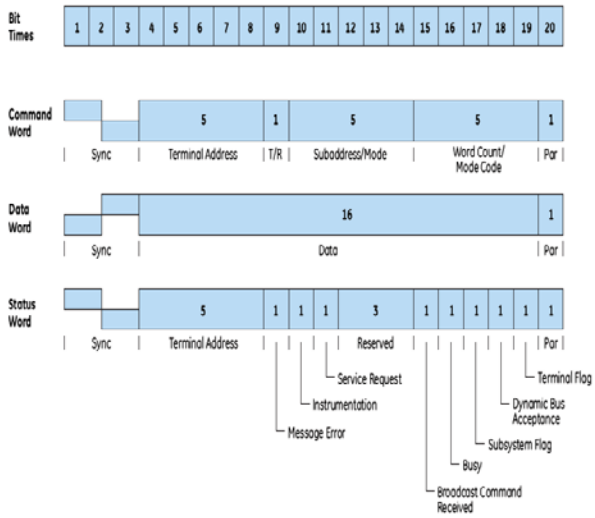

Fig 2 : Types of words.

The message formats can be sub divided into two types.

a) Non-broadcast message formats.
b) Broadcast message formats.

Non broadcast message formats are Bus controller to remote terminal, remote terminal to bus controller, remote terminal to remote terminal, mode command word with data word (transmit), mode command word with data word (receive), mode command without data word. Figure 3 shows different types of non broadcast message formats.

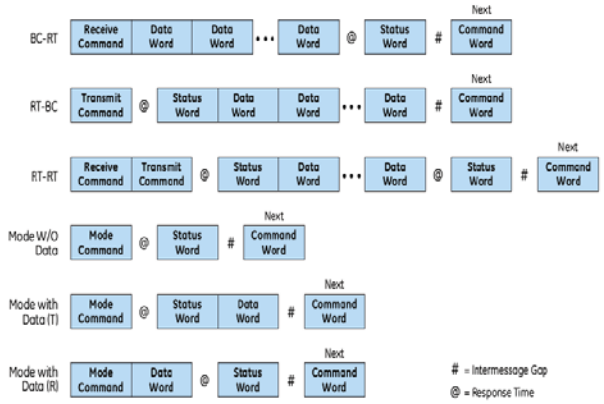

Fig 3: Non broadcast message formats.

Broadcast formats are bus controller to remote terminal transfer; remote terminal to remote terminal transfer, mode command without data word and mode command with data word (receive). Figure 4 shows broadcast message formats

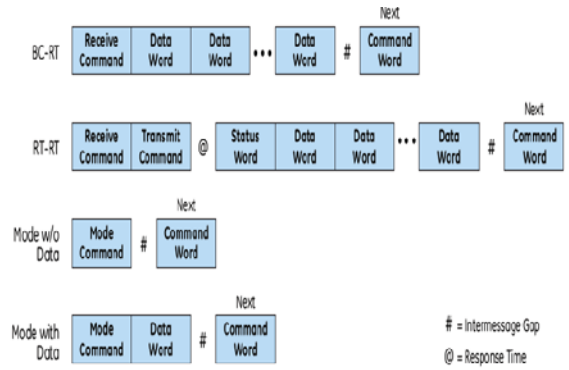

Fig 4: Broadcast message formats.

2. Architecture Description

According to the MIL-STD-1553B the functional architecture of the core is shown in figure 5. The following architecture can be used as bus controller, remote terminal or bus monitor.

The total design is sub divided in to several blocks. The CPU writes all the required commands and data into the RAM for each transmission. There by reducing the load and wastage of time of CPU as the clocks are different. The CPU gets interrupts from the interrupt handler, which takes care of informing the CPU regarding the completion of transmission, errors during transmission and status of the terminal. For a message retransfer command it simply gives commands to RAM instead CPU, thereby reducing

load on CPU. The interrupt handler Communicates with engine and takes signals, process them and produces required interrupts or commands.
The engine takes the bits from the registers block and produces enable, load, transmission and signals that are required for the remaining blocks. The engine gives the selection bits to the multiplexer depending on the bus activity. It gives the load signals to the register blocks. The engine also sets the mode of the core i.e. bus controller or remote terminal or bus monitor.

The host interface acts as Communication Bridge between the internal block and RAM; it passes the data on the RAM on to the internal data bus which is 16 bit wide. The internal data bus connects to internal registers and memory block. The registers block contains the control register, status register, error registers. Each register is 16 bit. The control register hold the control bits, the status register holds different status bits regarding transmission, memory block etc. The error contains the information of errors occurred.

The Tx memory block contains command registers which stores commands

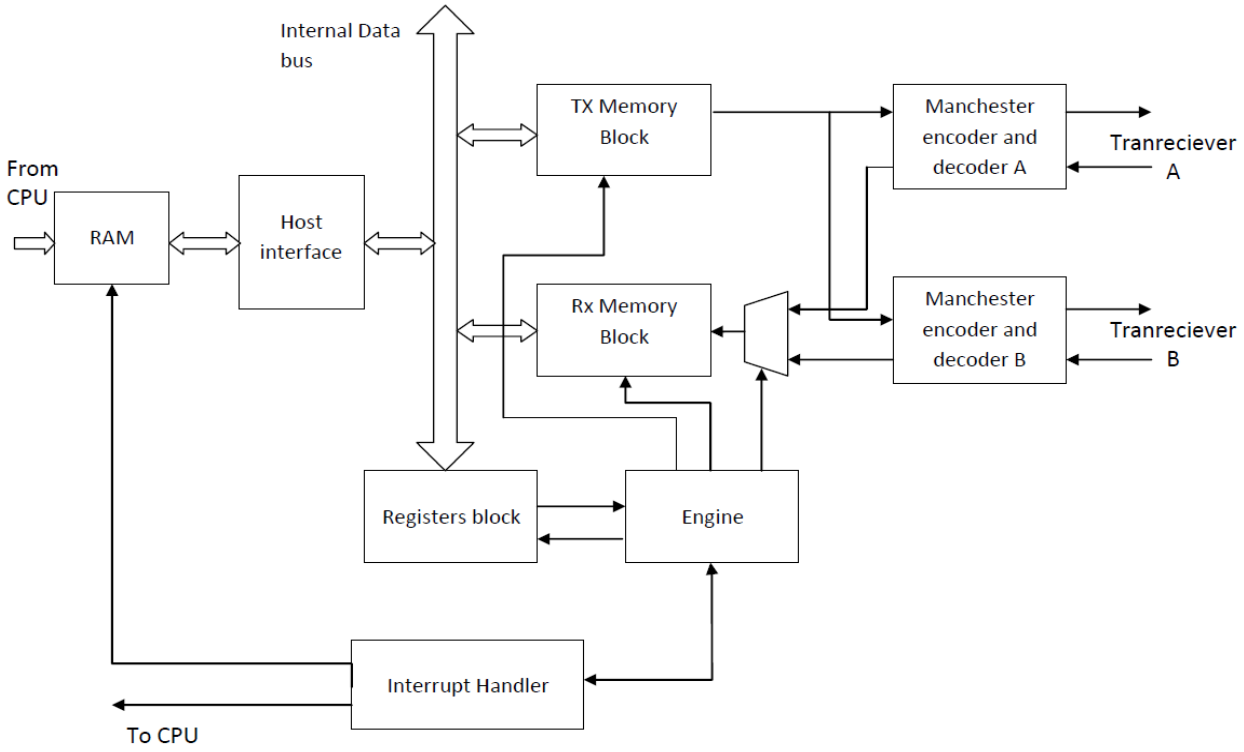

Fig 5: Architecture of the MIL-STD-1553B core.

to be transmitted during bus controller mode, status word register which stores the status words in remote terminal mode and FIFO that stores data to be transmitted. The Rx memory block contains the status word registers that stores the status words received for bus controller mode, command word registers for remote terminal mode and FIFO to store the data received on the buses.

The Manchester encoder and decoder encode the data and commands that are to be transmitted in to bi phase Manchester II format. The Manchester II format provides a self clocking waveform in which the bit sequence is independent. Similarly it decodes the messages received in bi phase Manchester II format. There are two Manchester encoder and decoders each for bus A and bus B. The data is received from the transreceivers that are connected to thebuses.

3. Implementation Results

The IP core of MIL-STD-1553 has been written using the verilog HDL and implemented in Xylinx vertex-2,Spartan-3 FPGA and it has used area of 891(4- LUT count).The output on the bus for different types of transmissions is shown in figure 6.

References

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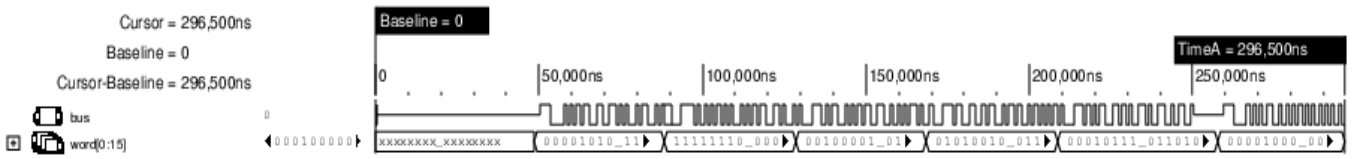
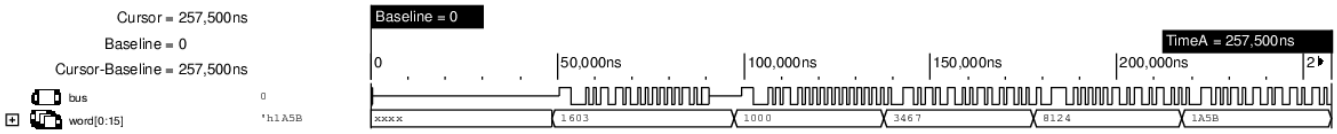
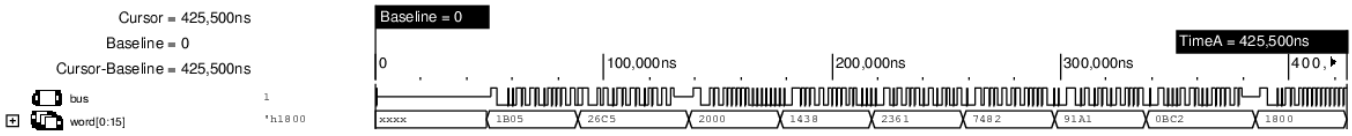


(a) BC-RT transmission waveform on the bus.



(b) RT-BC transmission waveform on the bus.



(c) RT-RT transmission waveform on the bus.

Figure 6: The waveforms on bus for different type's transmission, in Manchester II format.