An Efficient Switching Activity Reduction Technique for On-Chip Data Bus

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Abstract

In Deep-submicron (DSM) systems, the coupling effect on on-chip data buses and interconnects plays an important role in overall performance and reliability of the VLSI systems. In many digital processors and SoC the switching activity results into dynamic power dissipation on the data buses and interconnects which is a major part of the total chip power dissipation. Switching activity is due to self transitions and coupling transitions. Reducing the power dissipation of the VLSI chip is one of the major challenges in the DSM technology. One of the best techniques to reduce the transitions is to encode the data on the data bus. Hence an efficient switching activity reduction technique is proposed which can reduce the overall transitions. The proposed encoding technique reduces the coupling transition by 29% to 33%, self transitions by 4% to 19% and overall transitions by 22% to 27%. Its efficiency is 10% to 17% more compare to others encoding techniques.

Keywords: *Coupling transitions, Self transitions, VDSM, crosstalk, interconnects, SoC, Power dissipation.*

1. Introduction

As CMOS technology progresses into nanometer and sub-nanometer technology, it poses many challenges to design and test engineers. The scaling of VLSI integrated circuits has increased the sensitivity of CMOS technology to cause large power dissipation, propagation delays and various noise mechanisms such as power supply noise, crosstalk noise, leakage noise, etc. The power consumption and crosstalk has become a major concern because of continuing decrease in the minimum feature size and the corresponding increase in chip density and operating frequencies. Most of the power is being wasted on the data buses and long interconnects as dynamic power dissipation for charging and discharging of internal node capacitances and inter-wire capacitances.

In Non Deep submicron technology the load capacitance or the substrate capacitance (C_L) between wires to substrate is dominating factor. The coupling capacitance (C_C) is between parallel wires which is negligible compare to the load capacitance. Unfortunately in nanometer and sub nanometer technologies the coupling capacitance dominates the load capacitance and its magnitude is several times larger than load capacitance. The characteristics of data buses and long interconnects such as wire spacing [9], wire length, wire material, wire width, driver strength, coupling length and signal transition time, etc. influences the coupling effect. This increased coupling effect on on-chip buses and on long interconnects not only increase the power dissipation but also deteriorate the signal integrity due to the coupling capacitance. As a results these busses and interconnects becoming more sensitive and prone to errors caused by crosstalk and delay faults [17], [18], [19].Reducing the power dissipating transitions can also reduces the crosstalk and delay faults [12], [13].The coupling capacitance also depends upon the data dependent transitions and the coupling effect will increase or decrease depending upon the relative switching activity between adjacent bus wires [14].

On-chip data buses play an important role in reliable communication and high-performance chips. Power is consumed because of charging and discharging of a coupling and load capacitance due to transition of a signal on data bus. Reducing the transition activity or switching activity on the on-chip data buses is the one of the attractive way of reducing power dissipation. Switching activity on the data bus can be reduced by employing bus encoding techniques. Several bus encoding techniques have been proposed to reduce power consumption during bus transmission in literature. These techniques mainly relay on reducing the data bus activity by reducing the self transitions or reducing the coupling transitions. Reducing power dissipating transition by encoding the data on the

data buses leads to reducing the bus activity hence overall power consumption is reduced.

Over the past few years, a number of coding techniques have been proposed for reducing the transitions on a data bus. For data buses, one popular coding scheme is the bus invert coding technique proposed by Stan and Burleson [1]. In this method it compares the successive data bus values and determining if inverting a data on data bus word would results in fewer bit transitions than not inverting the word. This technique is suitable for uncorrelated data patterns and is based on the Hamming distance. It calculates the number of bits that change state from one data word to next data word. If the number of bit transitions is greater than the half of the total number of bus lines, then the inverted data is transmitted over the bus, other wise original data is sent. This method effectively reduces the maximum number of transitions to one half of the number of data bits. Other variants of the bus invert coding schemes include a decomposition approach [5] and partial bus coding technique [6].Both these techniques have an area overhead to determine the suitable partition of the data bus. In addition, the decomposition approach [5] can require up to p-1 extra lines on the bus where p is the number of partitions of the original data bus. The energy dissipated due to coupling capacitance is analyzed in [7], [8]. For instruction buses Gray code [2], T0 code [3], the Beach code [4] have been proposed which reduces the transitions there by reducing the power dissipation. Dynamic coding method takes even and odd line as bus sub-group and finds the coupling transitions and then invert the sub-bus group which decreases the coupling transitions [11]. Bus regrouping method divides the bus into small sub-groups and then regroups by taking bits from different subgroups [15]. In Novel Coding Technique the data bus is sub divided into even and odd bit groups. Hamming distance between even sub group, odd sub group, inverted data and present data is compared with the data on the bus respectively. The sub-group whose hamming distance is lesser that subgroup's data is inverted and transmitted with two redundant control bits for decodes purpose. One of the disadvantage of this technique is coupling transitions occurs due to redundant bits also [16]. In almost all above mentions methods only coupling transitions are considered and self transitions either neglected or can not be reduced. The proposed method by using Bus regrouping with Hamming distance considers the reduction of both coupling as well as self transition which results to a more save in power consumption.

2. Self and Coupling Transitions

Self transition on the data bus is defined as transition on the capacitance between a data bus line and the substrate. Coupling transition on data bus is defined as transition on capacitance between adjacent bus lines [8].Dynamic power consumption of data bus in CMOS technology in DSM technology is give by $P = (\alpha_l C_l + \alpha_c C_c) V^2_{dd} f$, where α_l is average self transition on the data bus, α_c is average coupling transition on the data bus, C_l is load capacitance, C_c is coupling capacitance, V_{dd} is operating voltage and f is operating frequency. In most cases, designers have no influence on C_l, C_c, V_{dd} and f. In general α ($=\alpha_l + \alpha_c$) is termed as Switching activity (α). Switching activity is the better parameter that can be controlled and optimized at high level design. By reducing the switching activity (i.e α_l and α_c) overall power consumption can be reduced.

A self transition is said to occur whenever a data bus wire makes a transition from 0 to 1 or from 1 to 0. When this occur the substrate capacitance either charges from GND to V_{dd} or discharge from V_{dd} to GND respectively. The coupling transition activity depends on the switching activity between two adjacent data bus bit lines which can be explained as follows. If the signals on data bus paths changes as (00→11 or 11→00) switching occurs in both of the adjacent wires but to the same resulting state. If the signals on data bus paths changes as (10→00 or 01→00 or 01→11 or 01→11) switching occurs in one of the adjacent wires but to the same resulting state. If (00→00 or 11→11) no switching activity occurs. In all above cases the power consuming transitions are zero and the dynamic power consumption is not effected by C_c. The transitions (00→01or 00→10 or 11→10 or 11→01 etc.) occurs when single line switching occurs and the resulting state is different from the other. In this case only one power consuming transition occurs and the dynamic power consumption is affected by C_c. The transitions (10→01 or 01→10) occur when both the adjacent wires change their states to opposite logic levels. In this case two power consuming transitions occur and the dynamic power consumption is effected by C_c [10].

3. Low Switching activity Scheme

The proposed encoding technique is based on the number of coupling transitions occurring on the data bus when a new data is to be transmitted. For a signal transmission through a two-wire bus, all transitions between possible bit patterns are shown in Table 1. In the following analysis assume n=32-bit data words. By using the following algorithm coupling transitions and self transitions can be reduced. The proposed algorithm for 32-bit Data bus is given as follows:

Let 32-bit data bus be represented by

$a_0\ a_1\ a_2\ a_3\ a_4\ a_5\ a_6\ a_7\ a_8\ a_9\ a_{10}\ a_{11}\ a_{12}\ a_{13}\ a_{14}\ a_{15}\ a_{16}\ a_{17}\ a_{18}$
$a_{19}\ a_{20}\ a_{21}\ a_{22}\ a_{23}\ a_{24}\ a_{25}\ a_{26}\ a_{27}\ a_{28}\ a_{29}\ a_{30}\ a_{31}$

1. Calculate the number of power consuming CT (coupling transitions) of the present bus data with the previous bus data.

2. Calculate the number of power consuming ST (Self transitions) of the present bus data with the previous bus data.

3. If CT >= (n/2) then
3.1 Consider the grouping of the present bus data. Arrange the data on the data bus as
Odd Group: $a_0a_2a_4a_6a_8a_{10}a_{12}a_{14}\ a_{16}a_{18}a_{20}a_{22}a_{24}a_{26}a_{28}a_{30}$
Even Group: $a_1a_3a_5a_7a_9a_{11}a_{13}a_{15}a_{17}a_{19}a_{21}a_{23}a_{25}a_{27}a_{29}a_{31}$
Note: here odd group means, data in odd bit positions, even group means data in even bit positions.
3.2(a): The Hamming Distance between odd group of present data and odd group of previous data is calculated. This is represented as OHD = Odd bits Hamming Distance
3.2(b): The Hamming Distance between even group of present data and even group of previous data is calculated. This is represented as EHD = Even bits Hamming Distance
3.3: Transmit the data by following the below conditions:
If OHD > EHD, flip the data in odd bit positions and append bit '1' on the left and bit '0' on the right side of the encoded data.
If EHD > OHD, flip the data in even bit positions and append bit '0' on the left and bit '1' on the right side of the encoded data.
If OHD = EHD, flip the entire data and append bit '1' on the left and bit '1' on the right side of the encoded data.

Step 4: If CT<n/2 is true then transmits the data as it is, append bit '0' on the left and bit '0' on the right side of the encoded data.

Step 5: Calculate the self transitions of transmitted encoded data with present transmitting encoded data.

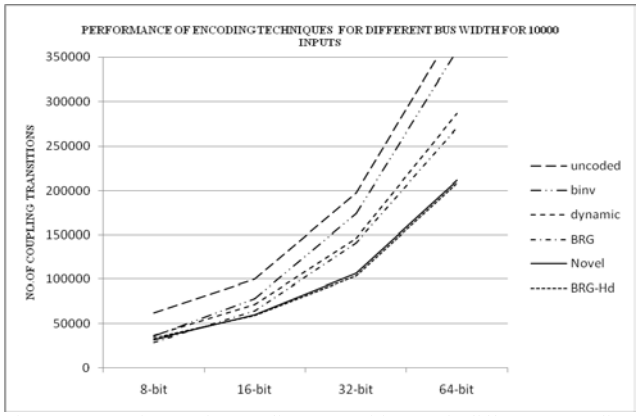

Fig.1: Comparison of Coupling Transitions of different encoding techniques with change of bus width.

Table 1: Margin specifications

Bit Pattern	00	01	10	11
00	0	1	1	0
01	0	0	2	0
10	0	2	0	0
11	0	1	1	0

4. Performance of the Proposed Technique

The effectiveness of proposed technique is evaluated by using a VHDL code. The simulations is performed on 8-bit,16-bit,32-bit and 64-bit data buses with three groups of 1000,2000, 5000 and 10000 data vectors. Self transitions and Coupling transitions are considered as metric parameters. Power consuming Self and coupling transitions are separately calculated for each method. The methods that are considered are Bus invert (Binv), dynamic, Bus regrouping (BRG), Novel and Bus regrouping with hamming distance (BRG-Hd).The performance of the techniques is evaluated by varying bus width and number inputs. Fig-1, Fig-2 and Fig-3 shows the performance variation of the different encoding techniques with respect to coupling transitions, self transitions and total transitions respectively. Bus invert [1] method is the best method to reduce the self transitions for all four bus widths. Bus regrouping method [15] is an efficient method to reduce coupling transitions for 8-bit data bus only. But as bus width increases its performance starts decreasing. This technique is best suitable for 8-bit data bus for reducing overall transitions. For 16-bit, 32-bit and 64-bit the proposed method is an efficient method to reduce coupling and overall transitions.

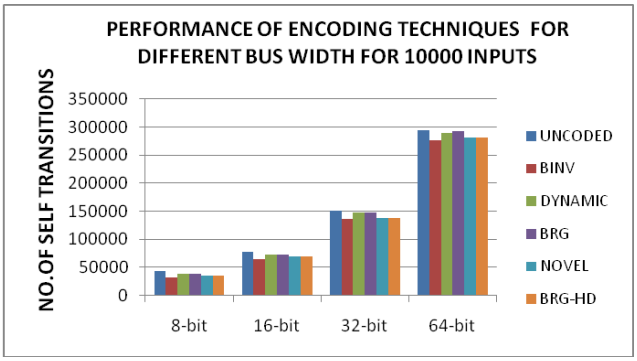

Fig. 2: Comparison of Self Transitions of different encoding techniques with change of bus width.

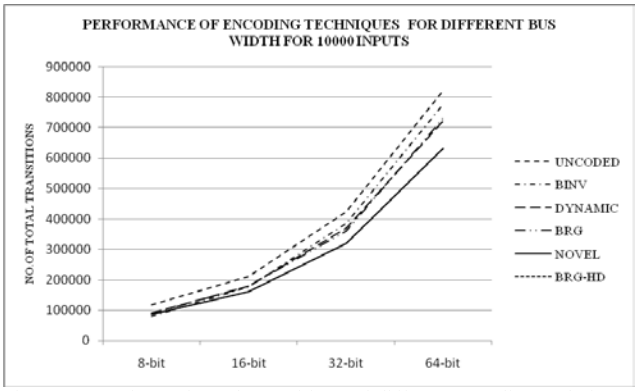

Fig.3: Comparison of Total Transitions of different encoding techniques with change of bus width.

The reduction in the number of coupling transitions achieved is high compare to that in the Bus invert, Dynamic, Bus Regrouping and Novel coding technique except for 8-bit bus. Fig-4, Fig-5 and Fig-6 shows that the proposed method is an efficient encoding technique to reduce the overall transitions. The proposed technique fails for 8-bit data bus as shown in Fig-7.

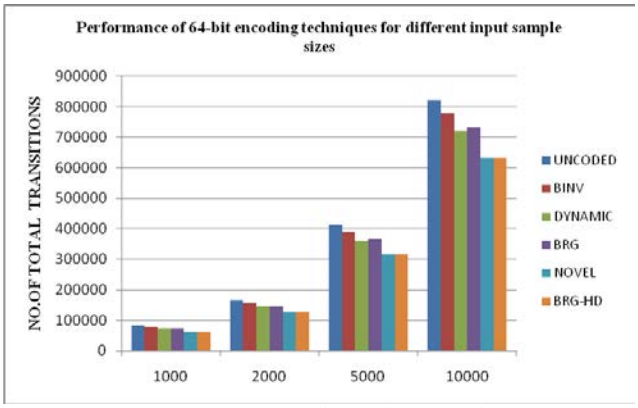

Fig. 4: Comparison of 64-Bit encoding technique with respect to Total Transitions

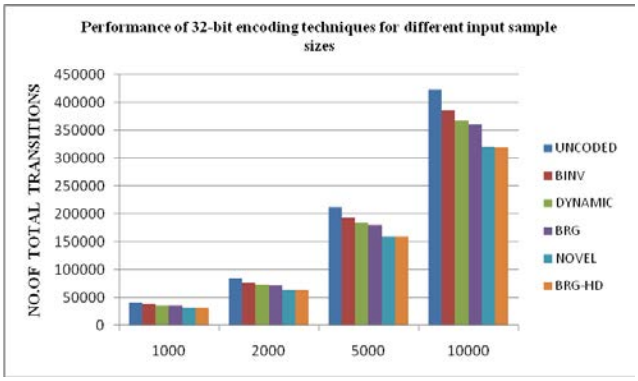

Fig.5: Comparison of 32-Bit encoding technique with respect to Total Transitions

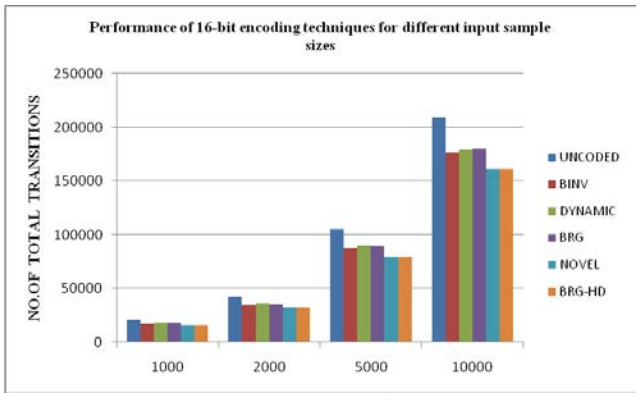

Fig-6: Comparison of 16-Bit encoding technique with respect to Total Transitions

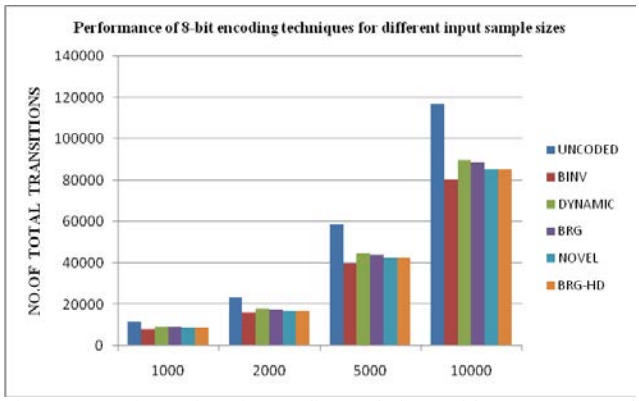

Fig.7: Comparison of 8-Bit encoding technique with respect to Total Transitions

Simulation results from the table 2, 3, 4 and 5 show that about 22% to 27% reduction in overall transitions is achieved by the proposed technique. Comparing with Bus invert, Dynamic, Bus Regrouping and Novel coding techniques proposed technique is 10% to 17% is more efficient. Since transitions are reduced, the power dissipation on the data bus can also be reduced. This intern reduces the crosstalk and hence error on the data bus.

The efficiency of different coding method is calculated by using the following formula:
Efficiency= (unencoded data – Coded Data) / Unencoded data x100
Here efficiency indicates how many coupling transitions are reduced after encoding with respect to the normal data.

TABLE 2: EFFICIENCY OF ENCODING TECHNIQUES FOR 64-BIT DATA-BUS

Method	Uncoded TT	Coded TT	Efficiency in %
BINV	822915	778069	5.4496515
	829041	784861	5.3290489
	828683	783465	5.4566101
DYNAMIC	822915	721777	12.290212
	829041	729785	11.972387
	828683	728288	12.115007
BRG	822915	732373	11.002594
	829041	731657	11.746584
	828683	730764	11.816219
NOVEL	822915	632562	23.131551
	829041	642472	22.504195
	828683	639529	22.825857
BRG-HD	822915	631599	23.248574
	829041	640871	22.697309
	828683	637934	23.018331

TABLE 3: EFFICIENCY OF ENCODING TECHNIQUES FOR 32-BIT DATA-BUS

Method	Uncoded TT	Coded TT	Efficiency in %
BINV	422923	386778	8.546472999
	423600	385819	8.919027384
	421314	385573	8.48322154
DYNAMIC	422923	367942	13.00023881
	423600	367833	13.16501416
	421314	367041	12.8818411
BRG	422923	360810	14.6865978
	423600	359059	15.23630784
	421314	359991	14.55517737
NOVEL	422923	320219	24.28432599
	423600	320395	24.36378659
	421314	323653	23.18009845
BRG-HD	422923	319102	24.54844026
	423600	319175	24.65179415
	421314	322513	23.45068049

TABLE 4: EFFICIENCY OF ENCODING TECHNIQUES FOR 16-BIT DATA-BUS

Method	Uncoded TT	Coded TT	Efficiency in %
BINV	209691	176951	15.61345027
	210447	177080	15.85529848
	209792	177137	15.56541718
DYNAMIC	209691	179126	14.57620976
	210447	179451	14.72864902
	209792	179887	14.25459503
BRG	209691	180422	13.95815748
	210447	179932	14.50008791
	209792	180188	14.11111959
NOVEL	209691	161027	23.20748148
	210447	161744	23.14264399
	209792	161965	22.79734213
BRG-HD	209691	161002	23.21940379
	210447	161412	23.30040343
	209792	161658	22.94367755

TABLE 5: EFFICIENCY OF ENCODING TECHNIQUES FOR 8-BIT DATA-BUS

Method	Uncoded TT	Coded TT	Efficiency in %
BINV	116961	80162	31.46262429
	116201	79837	31.29405083
	116296	80533	30.75170255
DYNAMIC	116961	89828	23.19833107
	116201	89569	22.91890775
	116296	89719	22.85289262
BRG	116961	88715	24.14993032
	116201	88544	23.80099999
	116296	89318	23.19770241
NOVEL	116961	85245	27.11673122
	116201	84668	27.13659951
	116296	85692	26.31560845
BRG-HD	116961	85277	27.08937167
	116201	84574	27.21749383
	116296	85762	26.25541721

5. Conclusions

Proposed efficient technique for data encoding scheme called Bus Regrouping with Hamming Distance method reduces the power consuming coupling transition a well as the self transitions on data bus transmission in deep sub-micron and very deep sub-micron buses. The main aim of the proposed technique is to reduce the overall transitions in DSM and VDSM technology which would leads to reduction in the dynamic power consumption by the on-chip data buses. The reduction in the coupling transition leads more power saving than reduction in self transitions in DSM technologies. This coupling capacitance also introduce errors in interconnects. Hence these errors can be reducing as the technique reduces power critical transitions. The simulation results show that the proposed technique reduces 29% to 33%of the power dissipating coupling transitions,4% to 16% power dissipating self transitions and its efficiency is 10% to 17% more compared to the Bus invert, dynamic coding, Bus Regrouping and Novel coding techniques in Deep sub-micron and Very deep sub-micron technology.

6. Future Scope of work

This inter-wire capacitance or coupling capacitance causes errors and delay faults in interconnects. Many techniques have come out to reduce the power dissipation. As the technology moves towards very deep submicron area the crosstalk is one of the main challenging problems which cause delay and error on the data bus. While attempting to reduce the power dissipation by using the coding techniques, it is a very important factor that these techniques should also consider the errors introduced due crosstalk and delay faults. Such a technique can be called as an efficient one. Hence the coding techniques can be found so that a considerable reduction in power dissipation and error correcting is possible. Our next work is to calculate the power consumed by the encoding and decoding circuit and compare with power saved due to the reduction of transitions and to evaluate its performance in the presence of errors due to crosstalk.

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