IJCSI International Journal of Computer Science Issues, Volume 15, Issue 1, January 2018
ISSN (Print): 1694-0814 | ISSN (Online): 1694-0784
www.IJCSI.org https://doi.org/10.20943/01201801.4851

A Novel Design and Implementation of new Peres and Six-Correction (PSCL) gate in Quantum-dot Cellular Automata (QCA) Technology

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Abstract

In recent years Quantum cellular automata (QCA) have been used widely to digital circuits and systems. QCA technology is a promising alternative to CMOS technology. It is attractive due to its fast speed, small area and low power consumption. The QCA offers a novel electronics paradigm for information processing and communication. It has the potential for attractive features such as faster speed, higher scale integration, higher switching frequency, smaller size and low power consumption than transistor based technology. In this paper, new Peres and Six-Correction (PSCL) gate is proposed based on QCA logic gates: the PSCL gate, MV gate and Inverter gate. The proposed circuit is a promising future in constructing of nano-scale low power consumption information processing system and can stimulate higher digital applications in QCA.

Keywords: *Quantum Cellular Automata; QCA Logic Gates; PSCL gate.*

1. Introduction

Quantum technology has gradually applied in various fields [1,2]. Quantum-dot cellular automata is projected as a promising nanotechnology for future ICs [3,4]. A QCA is an array of structures known as quantum-dots. Computing with QCA is achieved by the tunneling of individual electrons among the quantum-dots inside a cell and the classical coulomb interaction among them. A QCA cell consists of two electrons positioned at opposite corners owing to columbic repulsion, so the polarization states of P= -1 and P= +1 can be represented by two stable configuration of a pair of electrons, the corresponding the logic values of “0” and “1” also be represented in Fig. 1 The electrostatic repulsion between electrons leads to the synchronization of neighboring cells. Thus, one cell’s polarization is determined by the effect of its neighboring cell’s polarization.

Therefore, the array of QCA cells will be able to propagate information as a wire [5]. The QCA cells can form the primitive logic gates shown in Fig. 2 (inverter gate), Fig. 3 (majority gate). A majority gate with the logic function of MV(A,B,C) = AB+AC+BC is composed of five cells. By setting one of the inputs of this gate permanently to 0 or 1, AND and OR functions will be formed in QCA. Some other combinational logic designs with plus-shaped quantum-dot cellular automata using minority gate as the fundamental building block have been presented in [6].

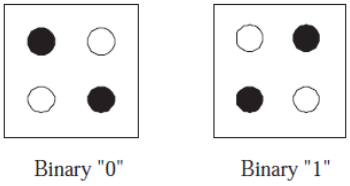

Fig. 1Quantum cellular automata

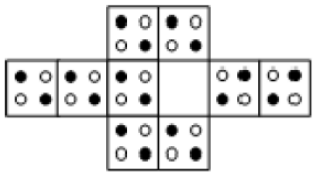

Fig. 2 Inverter gate

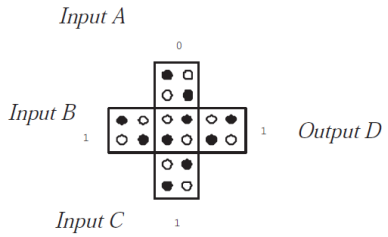

Fig. 3 Majority gate

An array of cells that are aligned can construct a QCA wire which is shown in Fig.4. The polarization of each cell in a QCA wire is directly affected by the polarization of its neighboring cells on account of electrostatic force. Accordingly, QCA wires can be used to propagate information from one end to another [7](Kim et al., 2007).(SCL Paper Reference)

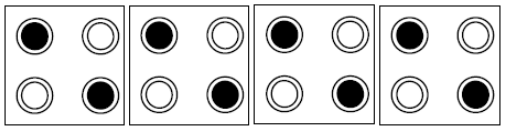

Fig. 4 A QCA Wire

2. Six-Correction Logic Gate

Six-Correction Logic Gate is a 4 x 4 gate with two garbage outputs [8] (Bhagyalakshmi, et al., 2010), the input vector is I (A, B, C, D) and the output vector is O (P, Q, R, S) and output is defined by P = A, Q = B, R = C, S=A (B+C) ⊕D the relation between input and output shown in Fig.5. There is a one-to-one mapping between inputs and outputs of SCL gate and it can be used to add 6 to the sum in order to correct it to get the correct BCD sum [8] (Bhagyalakshmi, et al., 2010).

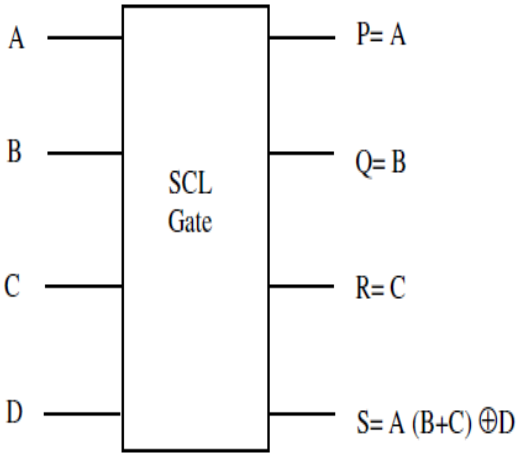

Fig.5 Six-correction logic gate (SCLG)

2.1 Double Feynman gate (F2G)

Fig.6 shows a 3x3 Peres gate [9]. The input vector is I (A, B, C) and the output vector is O (P, Q and R). The output is defined by P = A, Q = A⊕B and R=AB⊕C.

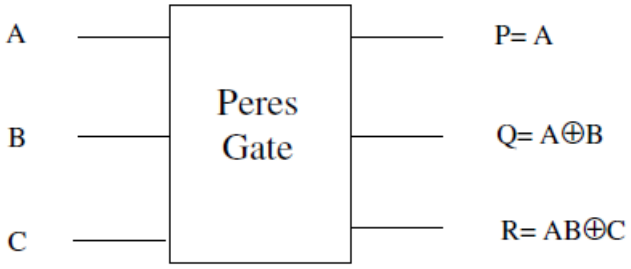

Fig.6 Peres gate

3. Proposed Peres and Six-Correction (PSCL) Gate

PSCL gate

Fig.7 shows a PSCL Gate. The input vector is I (A, B, C, D) and the output vector is O (P, Q, R, S).P =A, Q =A⊕B, R = C and S= A(B + C) ⊕D.

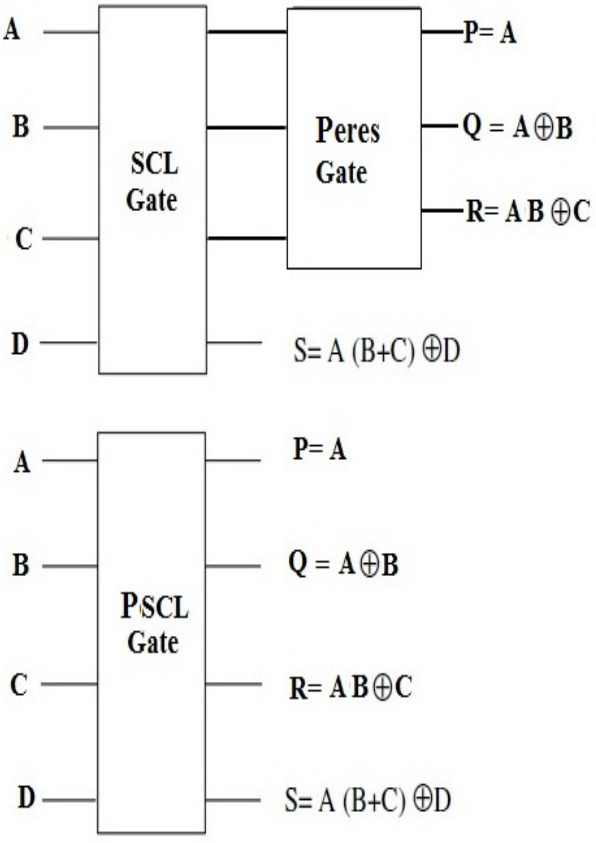

Fig.7 PSCL Gate

Fig.8 shows the QCA representation of Peres and Six-Correction Logic Gate (PSCL) based of majority voter (MV) gate. Here twelve majority voter gates are used to design Six-correction logic gate (PSCL).

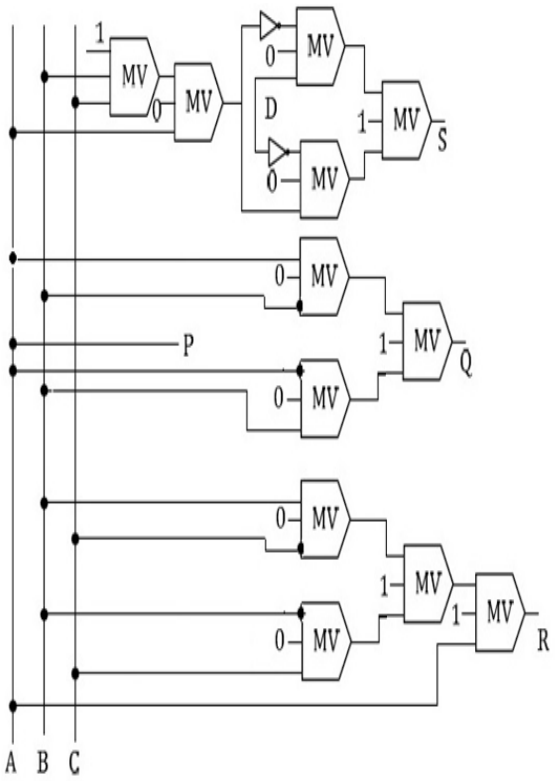

Fig.8 QCA block diagram of PSCL gate

4. Simulation and Result Discussion

The circuit is functionally simulated using the QCADesigner [10] (Walus et al., 2004). The simulated circuit layout is shown in figure 6, here the input signals are: A, B, C and D and the output signals are: P=A, Q=B, R=C and S=A (B+C)⊕D and this module goes through four clock zones, it means that the delay is a full clock cycle. Therefore, at the output P, Q, R and S are available one clock cycles after A, B, C and D has been applied. Moreover, it requires sixty one (61) cells and total area of 0.095 μm2.

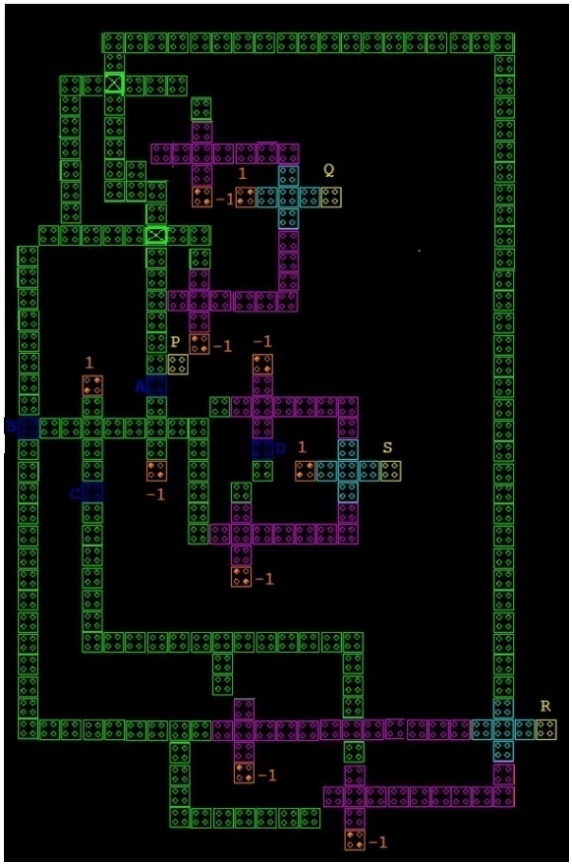

Fig.9 QCA circuit layout of PSCl logic gate

We can find the output value of S is low level when the input digits (A = 0, B = 0, C = 0, D = 0) and S is up level when the input digits (A = 0, B =0, C= 0, D =1). We look into the other two output values of A, B and C also translating the input data successfully. The simulated waveforms of PSCL gate is shown in Fig.10. Here, the S output is delayed by 0.75 clock cycle.

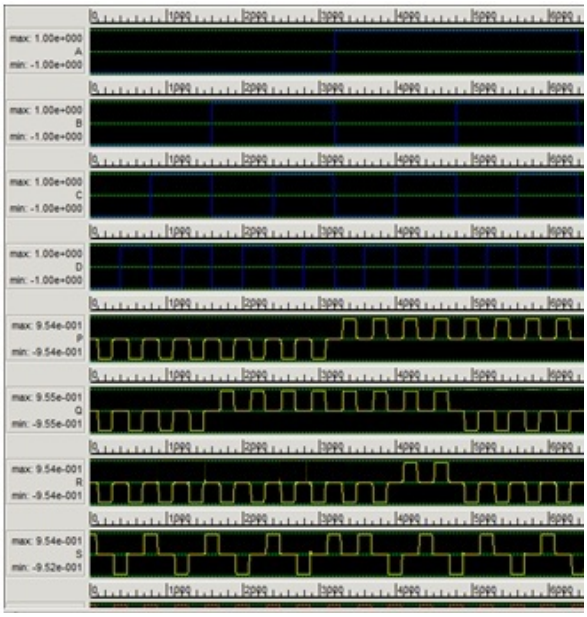

Fig.10 Simulated waveforms for PSCL gate circuit.

5. CONCLUSIONS

This paper present Peres and Six-correction logic (PSCL) gate based on QCA does logic gates. The proposed PSCL gate has been simulated and verified using QCADesigner. The result is compared in terms of complexity (cell count), covered area and time delay. The simulation result shows that the proposed design achieves a sound improvement. This design will be very helpful for designing ultra low power digital circuits.

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