IJCSI International Journal of Computer Science Issues, Volume 13, Issue 5, September 2016
ISSN (Print): 1694-0814 | ISSN (Online): 1694-0784
www.IJCSI.org https://doi.org/10.20943/01201605.2835

5T SRAM Cell with Improved Read/Write-ability and Reduced Standby Leakage Current

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Abstract

In this paper, a new single-port five-transistor (5T) Static Random Access Memory (SRAM) cell and associated read/write assist circuitries is proposed. Amongst them, a voltage level conversion circuit is to provide a voltage of the respective connected word line to be lower than or equal to a power supply voltage VDD such that the read/write-ability of the cell can be improved. Furthermore, a voltage control circuit is coupled to the sources corresponding to the driver transistors of each row memory cells. This configuration is aimed to control the source voltages of driver transistors under different operating modes. In addition, introducing a two-stage reading mechanism to increase the reading speed and thus to avoid unnecessary power consumption. Finally, with the standby start-up circuit design, the cell can rapidly switch to the standby mode, and thereby reduce leakage current in standby.

Keywords: *Static random access memory, Read/write assist circuitry, Voltage level conversion circuit, Voltage control circuit, Standby start-up circuit.*

1. Introduction

Recently, Static random access memory (SRAM) is used in a large variety of consumer electronics, such as computers and cellular phones. SRAM requires no refreshing and will maintain its information as long as it has sufficient power supplied. This is due to the fact that the SRAM cell includes flip-flop circuitry internally that does not require refreshing. However, it is apparent that SRAM suffers from the disadvantage of relying on too many transistors. Accordingly, there is an important need to have an SRAM cell that requires fewer than six transistors.

An SRAM cell has three modes of operation, namely read, write and standby [1]. The data stored in the cells may be corrupted when the cells are read. This problem arises from the fact that a higher voltage on the bit line is coupled to a lower voltage in the cell, causing the bit line voltage to drop and the cell voltage to rise. Further, a concern associated with the write operation is that it is relatively difficult to write a logic '1' to the cell if the cell currently stores a logic '0'. Accordingly, the SRAM cell should provide less likely to be corrupted when the cell is read and more reliable when the cell is written [2]. As integrated circuits become smaller and denser and as power consumption specifications for battery powered integrated circuits decrease, along with power supply voltages, the present SRAM cell designs are increasingly inefficient in both silicon area used and power consumed.

Memories take up 80% of the die area in high performance processors [3]. Therefore, there is a crucial need for a low leakage and highly robust SRAM design. Leakage current from a memory cell can cause unnecessary power consumption, especially during a standby mode. Recent research has shown that the leakage current will become even greater than the dynamic current in the overall power consumption [4]. Typically, there are three major sources of leakage in a MOS transistor, namely subthreshold leakage, gate leakage, and reverse bias junction leakage [5]. Amongst them, Gate-Induced drain leakage (GIDL) is an unwanted short-channel effect that occurs at higher drain biases in an overdriven off state of a MOS transistor. The GIDL is the result of a deep depletion region that forms in the drain at high drain-to-gate biases. However, Drain-induced barrier lowering (DIBL) is a short-channel effect in MOS transistors referring originally to a reduction of threshold voltage of the transistor at higher drain voltages. With scaling down of the MOS transistor, each of the leakage sources may increase accordingly, thus resulting in the increase of the total leakage current. As CMOS technology scales down to 90 nm and below, the power consumption caused by leakage currents is becoming a significant part of the global power consumption [6]. Therefore, it would clearly be desirable to provide a design for an SRAM cell that has less leakage current than traditional designs when the cell in standby.

The remainder of this paper is organized as follows. Section 2 presents a brief description of standard 6T and 5T SRAM cell topologies. The proposed 5T SRAM cell with integrated read/write assist is described in Section 3. The simulation results of the proposed 5T SRAM cell are discussed in Section 4. Last section is a conclusion and summary for the paper.

2. Existing 6T and 5T SRAM Cell Topologies

The standard 6T SRAM is built up of two cross-coupled inverters (INV-1 and INV-2) and two access transistors (MA1 and MA2), connecting the cell to the bit lines (BL and BLB), as shown in Fig. 1 [7]. The pair of cross-coupled inverters is formed by a pair of load transistors (MP1 and MP2) and a pair of driver transistors (MN1 and MN2) that are stronger than the access transistors. More specifically, the cross-coupled inverters of the memory cell have two storage nodes A and B functioning to store either logic '1' or logic '0'. The gates of access transistors are connected to a word line WL, and a rising transition on the word line to assert the access transistors during a read or a write operation. At the end of the read and write operations, the word line WL is de-asserted to allow the cross-coupled inverters to function normally and hold the logic state of the storage nodes.

A concern associated with the read operation is that because of the back-to-back connection of cross-coupled inverters, a regenerative action develops and node A is pulled high resulting in the destruction of contents in the bit cell. Especially, when a logic '0' stored initially, the voltage rise in the cell may corrupt the data stored. Therefore, it is desirable to keep the voltage at the storage node which has a logic '0' stored from rising above the trip-voltage of the inverter. To provide a non-destructive read operation, the cell ratio (CR) was conventionally varied from 1 to 2.5 [2], where the W/L ratio of the driver transistor to the access transistor is referred to as the cell ratio. Similarly, for a successful write operation, both access transistors must be stronger than the load transistors. The ratio of the load transistor to the access transistor is referred to as the pull-up ratio (PR). To improve the read-ability of an SRAM cell, cell ratio can be increased, while a lower pull-up ratio is desirable to improve the cell write-ability.

Figure 2 is a circuit diagram of a traditional 5T SRAM cell [8]. As shown in Fig. 2, the access transistor MA2 and bit line BLB in Fig. 1 have been removed to provide a five-transistor configuration. The removal of such access transistor allows for an area savings up to 20-30% compared to the standard 6T SRAM cell, while its power consumption is substantially reduced by one half [9]. Although the traditional 5T SRAM cells offer such significant reductions in power consumption, a serious drawback is presented in that it is difficult to write '1' to the cells. In detail, when the bit line BL is set high and the word line WL is asserted, the transistors MA1 and MN1 fight one another. To guarantee a correct write operation will occur, it is important to note that the storage node A must be pulled up (or down) above (or below) the trip-voltage of INV-2 within the word line WL is logic high, otherwise a write failure will occur. In more detail, writing a logic '1' to a cell when initially a logic '0' is stored, the low storage node A of the cell must be pulled up by the pre-charged bit line BL above the trip-voltage of INV-2. Undoubtedly, to properly write the wanted bit in the cell, it may be necessary that the access transistor should be very conductive to force the cross-coupled inverters to change its equilibrium condition. However, the access transistor should have a reduced conductivity for good stability in reading and standby operations. These two requirements impose contradicting requirements on cell transistor sizing.

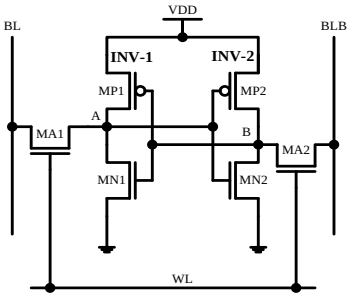


Fig. 1. Circuit diagram of standard 6T SRAM cell.

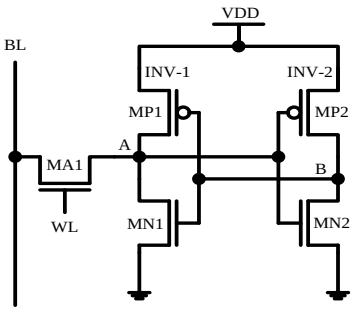


Fig. 2 Circuit diagram of traditional 5T SRAM cell.

As mentioned above, it is difficult to write '1' to a memory cell that is storing a '0'. In order to resolve the write '1' issue of the traditional 5T SRAM cells, several techniques have been developed. Some of these techniques rely on boosted word line voltage [10-12], reducing the supply voltage VDD [8-9], [13-14], sizing cell transistors [15-17], reduced bit line voltage [18-19], and raising the source voltage V_{SS} [20-22]. However, each of these techniques may cause a reduction in the drive current of the transistors and in the operating speed of the cell, or has increased memory cell area and a degradation in the manufacturing accuracy, or requires generation of a voltage above the operating voltage, or requires a more complicated circuit design and more complicated device process. Hence, there is a need for an effective technique to improve the write-ability of 5T SRAM cells which suffer from inability to write '1'.

3. The Proposed 5T SRAM Cell

3.1 The Proposed 5T SRAM Cell Configuration

The proposed 5T SRAM cell with read/write assist circuitries is shown in Fig. 3. Beyond memory arrays, there are read/write assist, namely level conversion circuit, pre-charging circuit, standby start-up circuit and voltage control circuit. Amongst them, the level conversion circuit receives an input signal WL and subsequently generates an output signal WLC that is lower than or equal to the power supply voltage VDD as shown in Fig. 4. The level conversion circuit is to provide a voltage of the respective connected word line when the respective word lines are in an active state. Unlike the traditional 5T SRAM cell in Fig. 2, a pull-down word line voltage is applied to the word line control signal WLC of a selected cell so as to improve the cell read- and write-ability. In detail, the level conversion circuit weakens the access transistor N13 such that the voltage drop across the transistor N13 increases and the voltage drop between the transistor N13 and the driver transistor N11 reduces, thereby increasing the read-ability. It is worth noting that the word line control signal WLC of the selected cell is provided a voltage VDD-V_{TN51} during a read operation, wherein V_{TN51} is the threshold voltage of the transistor N51. While, the power supply voltage VDD is supplied during a write operation. In addition, for each column in the SRAM array there is a bit line BL that connected to the pre-charging circuit. The function of the pre-charging circuit is to pull up the bit line BL of a selected column to VDD before the read or write operation. Furthermore, the standby start-up circuit design is to enable the SRAM cell to quickly switch to the standby mode, and thus effectively enhance the standby performance. When the standby control signal S is at logic low, the voltage of the node C will be equal to that of the inverse write control signal /WC. On the contrary, when the control signal S is at logic high, the voltage of the node C is zero. Thereby, in write '1' operation, to effectively avoid the control signal S transitions momently to a logic high caused by unexpected factors, and thus leads to a write failure. Wherein, in the non-read mode, the voltage of the read control signal RC is set to the voltage RGND to prevent the leakage current caused by the transistor N24 in the non-read mode. Furthermore, during the initial period in standby mode, the standby start-up circuit is designed to charge the parasitic capacitance of the node L1 to the voltage V_{TN23}. Finally, the voltage control circuit is connected to the source terminals corresponding to the driver transistors of each memory cell in a selected row cells. This configuration is intended to control the source voltages of the driver transistors under different operating modes.

Particularly, in this paper a two-stage read mechanism is introduced to speed up the reading speed and thus to avoid unnecessary power consumption during a read operation. Furthermore, during a write operation, the voltage V_{L1} is set to $V_{GS(N23)}$ and that of node L2 (V_{L2}) is set to the ground voltage, wherein $V_{GS(N23)}$ is the threshold voltage of the transistor N23. Thus, the issue concerning the difficulty of writing '1' can be resolved. In addition, during a standby operation, both V_{L1} and V_{L2} are set to $V_{GS(N23)}$ to reduce the leakage current in standby. Table 1 summaries the operating conditions under different operating modes.

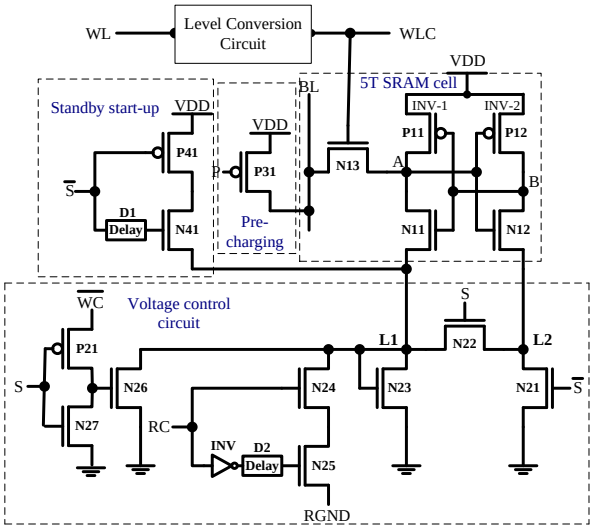
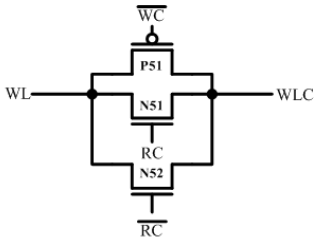


Fig. 3 Circuit diagram of the proposed 5T SRAM cell.



WL: Word Line; WLC: Word Line Control Signal
WC: Write Control Signal; RC: Read Control Signal

Fig. 4 Circuit diagram of the proposed level conversion circuit.

Table 1: The operating conditions under different operating modes

RC	WC	S	V_{L1}	V_{L2}	mode
RGND	0	0	$V_{GS(N23)}$	0	write
V_{DD}	0	0	RGND (1st stage) 0 (2nd stage)	0	read
RGND	0	V_{DD}	$V_{GS(N23)}$	$V_{GS(N23)}$	standby
RGND	0	0	0	0	hold

In Table 1, the write control signal WC can be achieved by performing the AND operation on the write signal W and its corresponding word line signal WL. And, the read control signal RC can be achieved by performing the AND operation on the read signal R and its corresponding word line signal WL.

An advantage of the proposed design over the traditional 5T SRAM cell is that it is unnecessary to boost the write line signal above VDD to speed up the read operation. Furthermore, this design has the additional advantage of increased current through the driver transistor during a read operation, and consequently lower read delay.

3.2 Write Operation

Refer to Fig. 3, prior to the write operation is performed, the standby start-up control signal S is at logic low and the inverse write control signal /WC is at logic high, thereby the transistors P21 and N26 are turned on and the transistor N27 is turned off, as such V_{L1} is pulled down to the ground voltage. However, during the write operation, both the signal S and the signal /WC are at logic low, thereby transistor N26 is turned off, as such V_{L1} is set to $V_{GS(N23)}$. Thus, the issue concerning the difficulty of writing '1' can be resolved. Figure 5 shows the simplified circuit diagram during the write operation.

The transients associated with a writing operation are detailed described below. Firstly, let us consider the write '0' operation. Prior to the write '0' operation, the voltage V_{BL} and signal WLC are at logic low. During the write '0' operation, if a '0' is stored previously, the signal WLC transitions from a logic low to a logic high. As the signal WLC exceeds the threshold voltage of transistor N13 (V_{TN13}), transistor N13 is turned on. Subsequently, owing to the fact voltage V_{BL} is at logic low, the voltage V_A remains at the ground voltage. On the other hand, if a '1' is stored previously, the signal WLC transitions from a logic low to a logic high. As the signal WLC exceeds the threshold voltage V_{TN13}, transistor N13 is turned on. Subsequently, owing to the fact voltage V_{BL} is at logic low, the node A and node L1 will be discharged to ground until the end of the write '0' operation.

Secondly, consider the write '1' operation. Prior to the write '1' operation, the signal WLC is at logic low and the voltage V_{BL} is at logic high. During the write '1' operation, if a '1' is stored previously, the signal WLC transitions from a logic low to a logic high. As the signal WLC exceeds the threshold voltage V_{TN13}, transistor N13 is turned on. Subsequently, owing to the fact voltage V_{BL} is at logic high and transistor P11 remains on, the voltage V_A will remain at the power supply voltage VDD until the end of the write operation. On the other hand, if a '0' is stored previously, the signal WLC transitions from a logic low to a logic high. Subsequently, with the increase of the signal WLC, the voltage V_A will rise. As the signal WLC exceeds the threshold voltage V_{TN13}, transistor N13 is turned on. Subsequently, owing to the fact voltage V_{BL} is at logic high and transistor N11 remains on, and the voltage V_B remains at a voltage close to the power supply voltage VDD, the transistor P11 remains off. For a successful write operation, it is desirable to pulling down the voltage V_A (or V_B) which has a stored value '1' below the trip-voltage of the inverter. Meanwhile, the write initial transient voltage V_{AW} of node A must satisfy the following equation:

$$V_{AW} = V_{DD} \times \frac{R_{N11} + R_{N23}}{R_{N11} + R_{N13} + R_{N23}} > V_{TN12} \quad (1)$$

where V_{TN12} is the threshold voltage of the transistor N12, R_{N11}, R_{N13} and R_{N23} are the on-resistance of transistors N11, N13 and N23, respectively. Consequently, the write '1' problem associated with the traditional 5T SRAM cell can be avoided.

Now, the transistor N13 is still in the saturation region and the transistor N11 in the triode region. Although R_{N13} may be greater than R_{N11}, the NMOS diode N23 can provide a voltage $V_{GS\ (N23)}$ at node L1. As a result, the voltage V_A will rise up due to the voltage division along the driver and access transistors. When the voltage exceeds a threshold, it causes the bit to flip due to regenerative feedback. Hence, the write '1' operation is completed. Consequently, the write '1' problem associated with the traditional 5T SRAM cell can be resolved. It is worth noting that the voltage V_{L1} is $V_{GS\ (N23)}$ when writing a logic '1' to a logic '0' is stored. After completing the write '1' operation, the voltage V_{L1} will be discharged to ground via transistor N26.

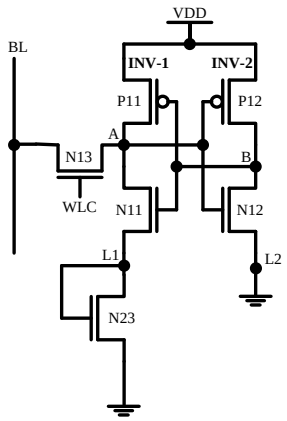


Fig. 5 Simplified circuit diagram during the write operation.

3.3 Read Operation

In this paper, a two-stage reading mechanism is introduced to increase the reading speed and thus to avoid

unnecessary power consumption. Figure 6 shows the simplified circuit diagram during the read operation. Prior to initiating a read operation, the bit line BL is pre-charged to VDD, the standby start-up control signal S, the write control signal WC and the read control signal RC are at logic low, thereby the transistors P13 and N25 are turned on and the transistors N24 and N27 are turned off, as such the voltage of node C is at logic high and subsequently turn on the transistor N26. This leads to the voltage V_{L1} will be pulled down to ground. In the first reading stage, the read control signal RC is at logic high, thereby transistor N24 is turned on. At this time, since transistor N25 would continue to conduct, V_{L1} will be pulled down to a negative voltage RGND as shown in Fig. 7. Under this circumstance, the negative voltage RGND can effectively improve the reading speed. However, in the second reading stage, the read control signal RC remains at logic high and the transistor N24 remains on. Consequently, V_{L1} is pulled up to the ground voltage due to the transistor N25 is turned off, and thus leads to reduce unnecessary power consumption. It is note that the two-stage time interval is measured as the time taken from a high on the read control signal RC to the state of the transistor N25 is turned off. This time interval can be adjusted by the falling time of the inverter INV and the delay time of the delay circuit D1. Furthermore, either in the first stage or in the second stage, the transistor N26 is always on.

The transients associated with a reading operation are detailed described below. Firstly, let us consider the read '1' operation. Before the read '1' operation occurs, the transistor N11 is off and the transistor N12 is on, and the voltage V_A and the voltage V_B are VDD and ground, respectively. And, the voltage V_{BL} is equal to VDD due to the pre-charging circuit. During the read operation, since the voltage V_{WLC} is VDD-V_{TN51}, the transistor N13 is turned on. Thereby the voltage V_{BL} can be effectively kept at VDD until the end of the read '1' operation. It is worth noting that due to the voltage RGND equaling to V_{L1}, in order to effectively reduce the half-selected cell disturbance and effectively reduce the leakage current during the read '1' operation, the absolute value of the voltage RGND may be set to be smaller than the voltage V_{TN11} in reading '1', i.e.,

$$|RGND| < V_{TN11} \tag{2}$$

where |RGND| denotes the absolute value of the voltage RGND and V_{TN11} is the threshold voltage of transistor N11. Secondly, consider the read '0' operation. Before the read '0' operation is performed, the transistor N11 is on and the transistor N12 is off, and the voltage V_A and the voltage V_B are ground and VDD, respectively. And, the voltage V_{BL} is equal to VDD due to the pre-charging circuit. During the read '0' operation, since the voltage V_{WLC} is VDD-V_{TN51}, the transistor N13 is turned on. Meanwhile, the initial transient voltage V_{AR} of the node A must satisfy the following equation:

$$V_{AR} = V_{DD} \times \frac{R_{N11} + (R_{N24} + R_{N25}) \| R_{N26}}{R_{N13} + R_{N11} + (R_{N24} + R_{N25}) \| R_{N26}} + RGND \times \frac{(R_{N11} + R_{N13}) \| R_{N26}}{R_{N24} + R_{N25} + (R_{N11} + R_{N13}) \| R_{N26}} \times \frac{R_{N13}}{R_{N11} + R_{N13}} < V_{TN12} \tag{3}$$

where V_{AR} is the initial transient voltage of node A, V_{TN12} is the threshold voltage of transistor N12, R_{N11}, R_{N13}, R_{N24}, R_{N25} and R_{N26} are the on-resistance of transistors N11, N13, N24, N25 and N26, respectively.

It is worth noting that, the voltage RGND is designed to be lower than the ground voltage and its absolute value is designed to be smaller than the voltage V_{TN11}. Furthermore, during the read '0' operation, the voltage V_{WLC} is set to VDD-V_{TN51} as in the paper. As such this design can be increased R_{N13} to satisfy the equation (3) and can reduce the half-selected cell disturbance in read '0' operation.

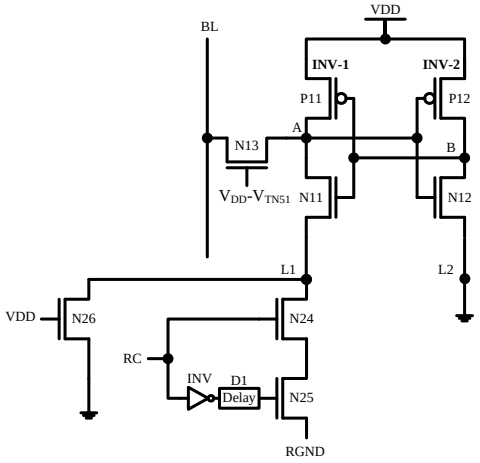


Fig. 6 Simplified circuit diagram during the read operation.

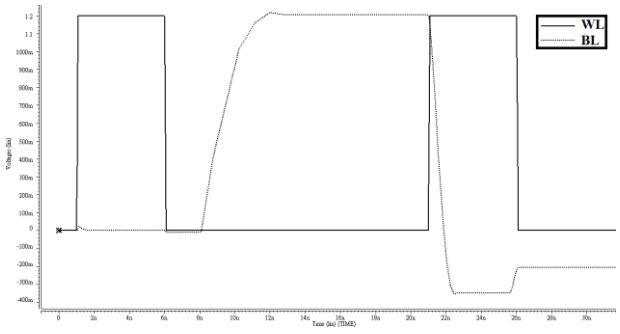


Fig. 7 Voltage level waveforms during a read operation.

3.4 Standby Operation

Refer to Fig. 3, prior to the standby operation is performed, the inverse standby control signal /S is at logic high and thus the transistor P41 is turned off and the transistor N41 is turned on. And then, during the standby operation, the signal /S is at logic low to turn on the transistor P41 and to turn off the transistor N21. In addition, the high standby control signal S is to turn on the transistor N22 which acts as an equalizer. Consequently, with the conduction of the transistor N22, both the V_{L1} and V_{L2} are equal to the voltage V_{TN23} as shown in Fig. 8. It is worth mentioning that node L1 can be rapidly charged to V_{TN23} at the initial period of the standby mode due to transistor N41 remains on, and thereby improving the standby efficiency. Note that the initial period is determined as the time taken from a low on the signal /S to the state of transistor N41 is off. This time interval can be adjusted by the delay time of the delay circuit D2. It is worth noting that after the initial period of the standby mode, transistor N41 is turned off and no current flows. Figure 9 shows the simplified schematic of the proposed design during the standby mode.

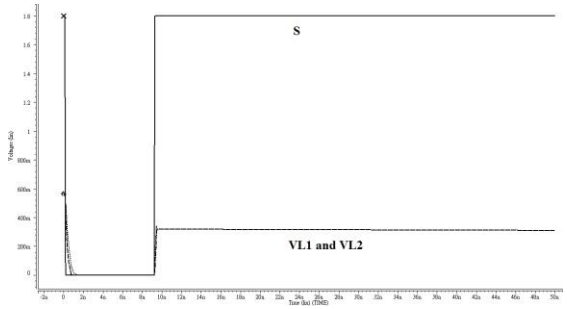


Fig. 8 Voltage level of node L1 and node L2 relative to the high standby control signal S

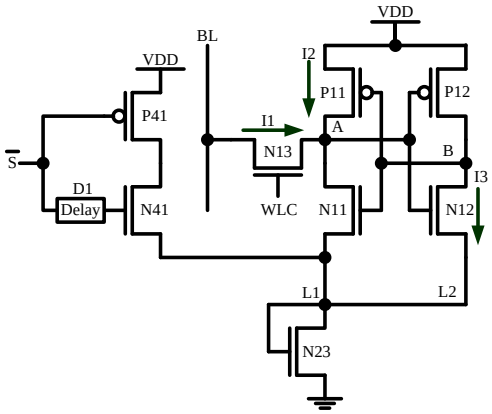


Fig. 9 Simplified circuit diagram during the standby operation.

4. Simulation Results

In this paper, the read operation is initiated by enabling the word line control signal WLC and connecting the pre-charged bit line BL to the storage node A. If the word line control signal WLC is reduced, the voltage V_A is also reduced during the read operation. In more detail, during the read operation, the word line control signal WLC in a selected row cell is set to a voltage VDD-V_{TN51}. Thereby, the gate voltage of the access transistor N13 of the selected cell is reduced to decrease its current driving power, and thus leads to prevent data corruption in the read operation. On the contrary, during the write operation, the word line control signal WLC in a selected row cell is set to a power supply voltage VDD, and the word line control signal WLCs for the non-selected row cells are set to a ground voltage similar to that in a read operation so that a static noise margin in the read operation is improved, and a write margin is ensured. Apart from these modes, the word line control signal WLCs for the non-access cells are set to a ground voltage.

In the traditional 5T SRAM cell, the access transistor MA1 is less conductive than the driver transistor MN1, thereby making it more difficult to write a logic ‘1’ to cell over a logic ‘0’ is stored. Figure 10 shows the simulated waveform of a write ‘1’ failure. To evaluate performance, different SRAM cell structures discussed in this paper were simulated using a 90nm CMOS technology. All simulations were carried out at nominal conditions: VDD=1.2V and at room temperature. The simulated waveform of a successful writing in the proposed 5T SRAM cell is shown in Fig. 11. It is evident that the proposed 5T SRAM cell provides an efficient solution to the write ‘1’ issue, that is, the proposed 5T SRAM cell enabling a logic ‘1’ to be easily written to the SRAM cell, as compared to the traditional 5T SRAM cells.

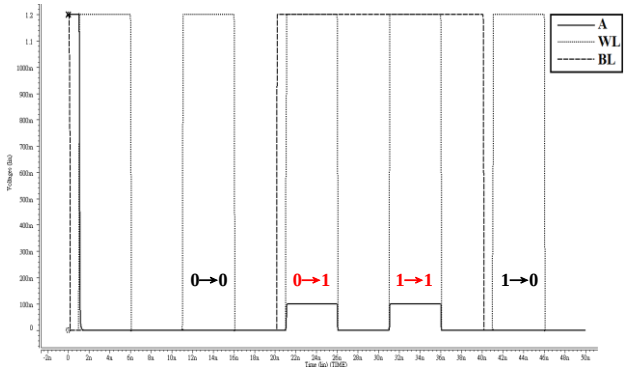


Fig. 10 Transient waveforms of a write failure in the traditional 5T SRAM cell.

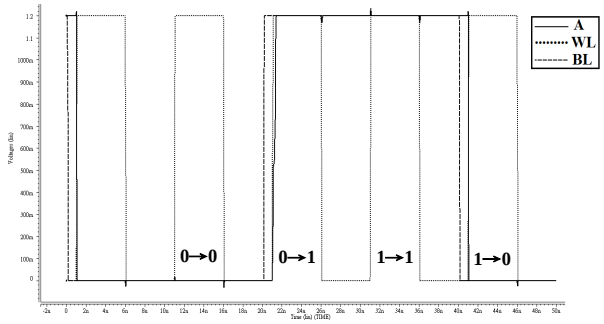


Fig. 11 Transient waveforms of a successful writing in the proposed 5T SRAM cell.

Table 2: Leakage current comparison

Corner model	Proposed 5T SRAM (pA)	Standard 6T SRAM (pA)	Improvement (%)
TT	2.0576	22.2203	90.7
SS	1.1091	1.6191	31.5
FF	39.3803	309.2402	87.3

Upon standby mode shown in Fig. 9, the voltage V_A remains at V_{TN23}, the voltage V_{WL} is set to the ground voltage and V_{BL} is set to VDD, respectively. Therefore, the gate-source voltage V_{GS} of transistor N13 is negative. In contrast, the V_{GS} of transistor MA1 in Fig. 1 is equal to zero. For NMOS transistors, according to the GIDL effect, the sub-threshold current at V_{GS}= -0.1 is approximately 1% of that at V_{GS}=0. Accordingly, the leakage current I1 flows through transistor N13 caused by the GIDL effect is much smaller than that of flowing through transistor MA1 in Fig. 1. Furthermore, the drain-source voltage V_{DS} of transistor N13 is VDD-V_{TN23}, whereas the voltage V_{DS} of transistor MA1 in Fig. 1 is VDD. According to the DIBL effect, the leakage current I1 flowing through transistor N13 is also less than that of flowing through transistor MA1 in Fig. 1. As a result, the leakage current flows through transistor N13 is much smaller than that of flowing through transistor MA1 in Fig. 1. Next, the source-drain voltage V_{SD} of transistor P11 is VDD-V_{TN23} in contrast to the V_{SD} = VDD of transistor MP1 in Fig. 1. According to the DIBL effect, the leakage current I2 flowing through transistor P11 will be less than that of flowing through transistor MP1 in Fig 1. Thus, the base-source voltage V_{BS} of transistor N12 is negative, and the drain-source voltage V_{DS} of transistor N12 is VDD-V_{TN23}. On the contrary, the V_{BS} of transistor MN2 in Fig. 1 is zero, and the V_{DS} of transistor MN2 is VDD. According to the body effect and DIBL effect, the leakage current I3 flows through transistor N12 is much smaller than that of flowing through transistor MN2. From the above analysis, it can be seen that the proposed 5T single-port SRAM having a lower leakage current compared with the standard 6T SRAM. Table 2 shows a comparison of the simulated standby leakages of the traditional 6T SRAM cell and the proposed 5T SRAM cell using 90 nm CMOS technology. For each cell, the total leakage current flow, which is the sum of I1, I2 and I3 of all transistors are estimated.

As it can be seen from Table 2, compared with the standard 6T SRAM cell in different corner models, the standby leakage current of the proposed design is significantly reduced 90.7%, 31.5% and 87.3%, respectively.

5. Conclusions

This paper facilitates efficient data reading from and writing to an SRAM cell, particularly if a logic ‘0’ stored in the cell is to be overwritten by a logic ‘1’. With the level conversion circuit limits a word line voltage to a value lower than the supply voltage of the proposed 5T SRAM cell to improve the read-ability and write-ability is used in simulations. Simulation results for the proposed 5T cell design confirm that there is conspicuous improvement over the standard 6T SRAM cell while it allows writing ‘1’ on the cell with read/write assist. In addition, with the proposed write assist leads to a 90.7%, 31.5%, and 87.3% less standby leakage in different corner compared with the standard 6T SRAM cell.

References

[1] N. H. E. Weste and D. M. Harris, CMOS VLSI Design: A Circuits and Systems Perspective, Addison Wesley, 2011.
[2] K. Itoh, *VLSI Memory Chip Designs*, Heidelberg, Springer-Verlag, 2001.
[3] M. Horowitz, “Scaling, power, and the future of MOS,” in *Proc. IEDM Tech. Dig.*, 2005, pp. 9-15.
[4] N. S. Kim, *et al.*, “Leakage Current: Moore’s Law Meets Static Power,” *IEEE J. Computer*, vol. 36, no. 12, pp. 68-75, Dec. 2003.
[5] D. A. Hodges, H. G. Jackson, and R. A. Saleh, *Analysis and Design of Digital Integrated Ciruits: In Deep Submicron Technology*, 3rd ed., New York: McGraw-Hill Press, 2004.
[6] J. Rabaey, A. Chandrakasan, and B. Nikolic, *Digital Integrated Circuits: A Designer Perspective*, 2nd ed., Upper Saddle River, NJ: Prentice-Hall, 2003.
[7] H. Tran, “Demonstration of 5T SRAM and 6T Dual-Port RAM Cell Arrays,” in *Proc. 1996 Symp. VLSI Circuits Dig. Tech. Papers*, 1996, pp. 68-69.
[8] I. Carlson, S. Andersson, S. Natarajan, and A. lvandpour, “A high density, low leakage, 5T SRAM for embedded caches,” in *Proc. ESSCIRC 2004*, Sept. 2004, pp. 215-218.
[9] S. Nalam and B. H. Calhoun, “5T SRAM With Asymmetric Sizing for Improved Read Stability,” *IEEE J. Solid-State Circuits*, vol. 46, no. 10, pp. 2431-2442, Oct. 2011.

[10] S. Nalam, V. Chandra, C. Pietrzyk, R. Aitken, and B. Calhoun, "Asymmetric 6T SRAM with two-phase write and split bit line differential sensing for low voltage operation," in *Proc. 11th Int. Symp. Quality Electronic Design (ISQED)*, Mar. 2010, pp. 139-146.
[11] Y. H. Chen, *et al.*, "A 0.6V 45nm adaptive dual-rail SRAM compiler circuit design for lower VDD_min VLSIs," in *Proc. IEEE Symp. VLSI Circuits*, June 2008, pp. 210-211.
[12] Y. Chung and S. H. Song, "Implementation of low-voltage static RAM with enhance data stability and circuit speed," *Microelectronics Journal*, vol. 40, no. 6, pp. 944-951, 2009.
[13] M. Yamaoka, *et al.*, "Low-power embedded SRAM modules with expanded margins for writing," in *Proc. IEEE Int. Conf. Solid-State Circuits (ISSCC 2005)*, Feb. 2005, pp. 480-611.
[14] H. Pilo, *et al.*, "An SRAM design in 65nm and 45nm technology nodes featuring read and write-assist circuits to expand operating voltage," in *IEEE Symp. VLSI Circuits*, 2006, pp. 15-16.
[15] K. J. O'Connor, "A source sensing technique applied to SRAM cells," *IEEE J. Solid State Circuits*, vol. 30, no. 4, pp. 500-511, Apr. 1995.
[16] M. H. Tu, J. Y Lin, M. C. Tsai, S. J. Jou, and C. T. Chuang, "Single-Ended Subthreshold SRAM With Asymmetrical Write/Read-Assist," *IEEE Trans. Circuits and Systems- I: Regular Papers*, vol. 57, no. 12, pp. 3039-3047, Dec. 2010.
[17] M. C. Shiau, C. C. Yu, and K. T. Chen, "Single port SRAM having a lower power voltage in writing operation", TW pat. I426514 B, Feb. 11, 2014.
[18] D. P. Wang, *et al.*, "A 45nm dual-port SRAM with write and read capability enhancement at low voltage," in *Proc. IEEE Int. SOC Conf.*, Sept. 2007, pp. 211-214.
[19] K. Nii, *et al.*, "A 45-nm single-port and dual-port SRAM family with robust read/write stabilizing circuitry under DVFS environment," in *Proc. IEEE Symp. VLSI Circuits*, June 2008, pp. 212-213.
[20] K. Kim, J. J. Kim, and C. T. Chuang, "Asymmetrical SRAM cells with enhanced read and write margins," in *Proc. Int. Symp. VLSI Technology, Systems and Applications (VLSI-TSA)*, Apr. 2007, pp.1-2.
[21] A. Bhavnagarwala, *et al.*, "Fluctuation limits & scaling opportunities for CMOS SRAM cells," in *Proc. IEEE Int. Electron Devices Meeting (IEDM 2005)*, Dec. 2005, pp. 659-662.
[22] H. S. Yang, *et al.*, "Scaling of 32nm low power SRAM with high-K metal gate," in *Proc. IEEE Int. Electron Devices Meeting (IEDM 2008)*, Dec. 2008, pp. 1-4.

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