Modeling Methodology for NoC: MM4NoC

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Abstract

The current technology allows the integration on a single chip of complex systems "SoC" which are composed of pre-designed blocks "IPs" that can be interconnected by a network on chip "NoCs. Generally, the IPs are validated by various techniques "simulation, test, formal verification" and the main problem remains the validation of communications infrastructure in order to compare the performance - latency, throughput, power consumption, area occupied.

Based on the work done in [1] that focuses on the formal verification of networks on chip using an automatic proof tool, this article presents a draft introduction to behavioral modeling and simulation of a communication network on chip.

Keywords: *communication network on chip, Multiprocessing, on-chip, N-dsp, N-core system.*

1. Introduction

This article provides an introduction to modeling and behavioural simulation of a communication network on chip "NoC - Network on Chip" [3].

The rapidly changing and increasingly complex systems on a chip "SoC - System on Chip" to SoC multi-processor "MPSoC - Multiprocessors SoC" interconnection communication modules or cores constituting these systems has undergoes a topological and structural change.

The latter meets the constraints of performance and cost related to the complexity and the increasing modules or interconnected cores. Currently this trend is moving towards the integration of on-chip communication network, implementing the transmission of packet data to the interconnected network nodes and corresponding to the "processor modules, memory controllers, connected devices,... "

The transmission of data is done through routers constituting the network and implementing rules switching and routing packets across the network [2].

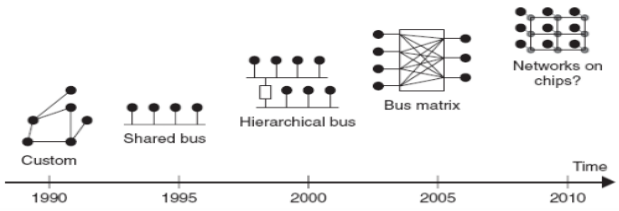


Fig. 1 Evolution in the interconnected SoC

2. Description environment of a NoC

2.1 Description NoC

Regarding technology, the term most commonly used is that of network-on-chip " NoC abbreviated as" derived from system-on-chip "SoC". While applications such as network on silicon or on chip network are rarely used.

Research on network-on-chip integrates various fields of development.

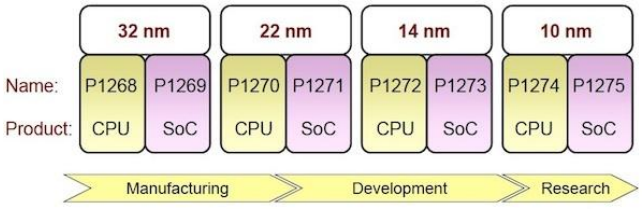


Fig. 2 NoC: from research to industrial use (By [7]).

Currently, all aspects of NoC have not yet been addressed and there is no industrial solution with a level of maturity comparable to the bus. NoCs are still at the research **Fig.2**.

One of the major advantages of on-chip networks is to provide a reliable and efficient interconnection structure to rapidly develop new routes from reusable building blocks, previously developed and validated, which provide a system for exchanging data between different processing resources: processors, memory, DSP "Digital Signal Processor" or cores...

2.2 Topology network interconnection

There are a wide variety of network topologies [3], whether direct or indirect, regular or irregular. Obviously, the list of topologies that follows is not exhaustive but represents those most often used in NoCs.

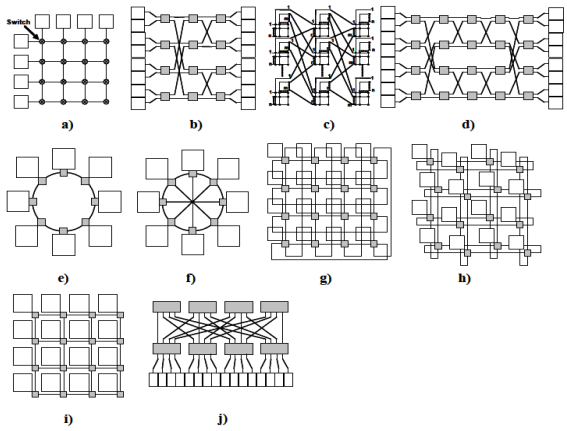
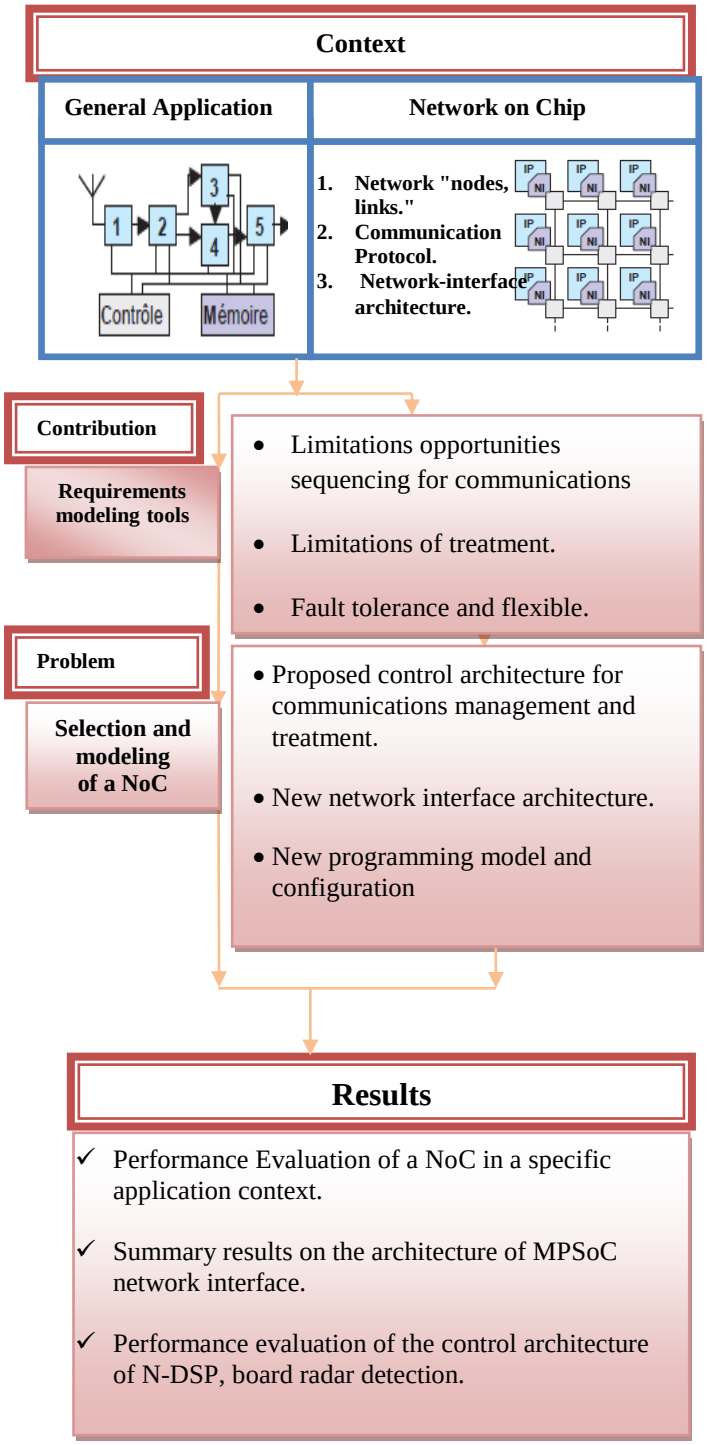


Fig. 3 Topologies often used in Nocs: (a) crossbar (b) Buttery (c)Clos (d)Benes (e) ring (f) chordal ring (g) torus (h) folded torus (i) 2D mesh (j) fat tree. **[3]**

Network interfaces and routers can be configured to optimize communication paths of data flows exchanged through the NoC. There are several examples of network-on-chip: STNoc , SPIN , Xpipes , Hermes, FAUST Æthereal

3. Diagram of Research

This part of research is the study and modeling of a network on chip. architecture in the context of the implementation.



MODELING THE NOC, It models the behaviour of the communication network of independent processing units that will use this network. Several approaches are possible:

3.1 Use modeling environment high-level

The goal is to quickly develop a working model without the level of detail required for a physical implementation. These environments provide a set of primitives to build a system and simulate it. Include work done with Ptolemy [10] as SSMK01[12] and ZhMa02[13] or SDL [11] "specification and description language" for [6] and [5]. Overall, these environments are less used because they are not known in the middle of the design.

Most designs are planned and written in VHDL designed to be implemented directly on a chip usually a CPLD or FPGA.

3.2 Use a tool for modeling network

A solution to simulate a network on chip architecture is to take standard tools. Several network simulators are available and can be adapted to the problems of NoC. E.g. ModelSim [8], OPNET [9].

3.3 Develop a specific model

The approach most often chosen to simulate the operation of a network on chip is to develop a specific model of the architecture is designed from description languages or programming standards in order to have a model specific cycle or even the bit level to create an interconnection network onboard FPGA interconnects N-DSP of N-core in a MPSoC platform.

4. Evaluating the performance of NoC

4.1 General methodology

We distinguish four distinct phases: modeling (representing the behaviour of the system), programming, testing and interpretation of results (with shares).

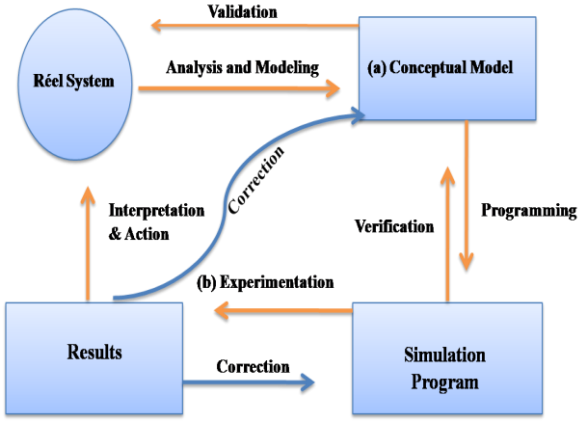


Fig. 4 Methodology adapted

- (a) **Conceptual Model:** The model is only an approximation of the system; it is conditioned by the objective of the study.
- (b) **Experimentation:** This build theories or assumptions that take into account the observed behaviour.

4.2 Implementation and performance analysis

CASE STUDY: achieve an interconnection network between four DSP chips Tms320c6474 three cores each and as much memory [4] different testing capabilities offered by this device to make. The platform has a CPLD future location of a NOC. [4bis]

At the beginning the study is to carry forward two DSP cores of two different but on the same map simulation, the result is a transfer pack data 256 bytes, via "The C6474 Evaluation Module" software.

5. Conclusions

This study modeling, simulation and communication network on chip architecture assessment to raise the fundamental role on the performance of interconnected systems expected in a MPSoC platform in its design.

The object is on the one hand the development and design of microelectronic interconnects, constituting the key performance of a multiprocessor platform, secondly, to show the value of using modeling tools allowing the simulation in order to test and validate an environmental architecture in its operating environment.

Indeed, the development of systems that are becoming more complex with the integration of both hardware and software parts, the technical co design.

The idea to connect and communicate several processor cores in a chip, which is a cross-disciplinary work

"Networks, Nanotechnology, Embedded Systems and Digital Communications " is:

- A reliable solution for modeling on-chip communication networks.
- A prototyping methodology based reconfigurable circuits (ie FPGA / CPLD) for rapid validation of systems design.
- Build on the results across multiple applications.

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