Architecture Exploration of Multicore Systems-on-Chip using a TLM-based Framework

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Abstract

A framework for TLM architecture exploration of multi-core systems is presented. Starting with a Task Precedence Graph (TPG) as a design entry, different architectures with different number of processor cores, number of busses, task-to-processor and channel-to-bus mappings are automatically generated. The viability and potential of the proposed approach is demonstrated by an illustrative example.

Keywords: *TLM, SoC, Architecture Exploration, Multi-Core*

1. Introduction

With the increasing complexity of multi-core systems, it is necessary to have an easy, efficient, and automatic technique for fast analysis of architecture trade-offs in early stages of the design [1]. Transaction Level Modeling (TLM) provides a fast, simple and powerful methodology to enable early exploration of possible architectures [2].

Several TLM-based design space exploration methodologies for multi-core systems have been developed. MULTICUBE presents a framework for design space exploration of multi-core systems based on design parameters [3]. The multi-processor platform is simulated based on Cycle Accurate (CA) TLM. The system requires an architect engineer to explore different strategies, metrics and constraints. The research in [4] targets the architecture exploration of inter-subsystem communication in Multiprocessor Systems-on-Chip MPSoCs with A Kahn Process Network (KPN) as the design entry. A Virtual Platform (VP) level, where software is executed by Instruction Set Simulators (ISS) and hardware cores are modeled using CA models, is adopted. CA modeling slows-down simulation which increases the time-to-market.

In this paper, a new Approximately-Timed (AT) TLM-based framework for architecture exploration of specialized multi-core system architecture is presented. Starting from Task Precedence Graphs (TPG) different architectures are explored. The presented technique allows visualization and easy analysis of throughput, latency, and utilization metrics of various resources in the system.

2. TLM Multi-Core Architectural Exploration Framework

The proposed framework for TLM-architecture exploration of specialized multi-core system architecture is shown in Figure 1. The design entry is the software application specified as a set of communicating tasks exchanging data through blocking channels expressed as a Task Precedence Graph (TPG).
A scheduling algorithm [5] is applied to solve the task allocation/scheduling problem to obtain the optimum schedule on a multiprocessor system while reducing the number of processors in the target system. The algorithm also resolves conflicts in the communication channels. The algorithm provides different architecture options [modeled as Architecture Level Models (ALM)] that satisfy the optimum schedule length with different number of processor cores. Each ALM represents an architecture structure of the system which is specified by the number of cores, the number of busses, task-to-core mapping, and channel-to-bus mapping.

Once the ALM file is generated, the target multi-core system and its simulation dynamics are automatically built using scalable transaction-level modeling methodology [6]. Functionality, communication, timing, and power are all separated aspects in the presented methodology. Each processor core has Local Memory (LM) that is used for the communication among the tasks on the same core. Each CPU core is the initiator for the required read/write transactions based on the running tasks. The tasks communicate using the shared memory through specific memory addresses. All models are instantiated from a library of fast generic models.

Each CPU core is modeled using a single SC_THREAD that runs different tasks according to the provided schedule. For each task, the thread is suspended for the specified execution time based on the computation cost of the running task. State-based power [7] is used to model the computational power for tasks which are running on each processor core. A state variable is changed whenever a new scheduled task start running on the core. The power consumption is evaluated

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based on the value of this state variable and is updated each time this state variable is refreshed.

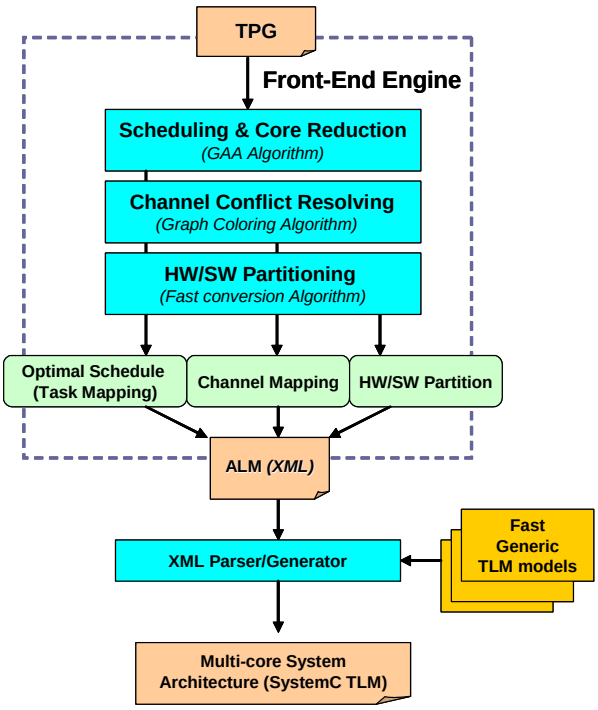
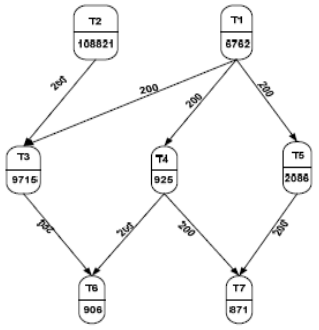


Fig. 1 TLM multi-core system architecture exploration framework.

3. Illustrative Example

A practical example is shown in Figure 2. The tasks computation cost as execution time in cycles and consumed energy in nJ are listed. The communication time for all communication channels is 200 cycles with energy consumption of 38µJ per bit. The scheduling algorithm provides two ALM models using two-core and three-core architectures with the same schedule length. A single core system was not sufficient to achieve the target latency.

The task mapping is illustrated for both architectures as shown in Figure 3. For the three-core architecture, two buses are needed to resolve the channel conflicts (Ch1 conflicts with Ch3 and Ch2 conflicts with Ch4). Using graph coloring algorithm, channels Ch1 and Ch2 are mapped to Bus1 and channels Ch3 and Ch4 are mapped to Bus2. The TLM-based architecture of the 3-core and the 2-core systems are plotted in Figure 4.



Tasks Profile

Task	Computation cost	
	Time (cycles)	Energy (nJ)
Sort (T1)	6762	571.74
Fir2d (T2)	108821	8455.4
Mat1XN (T3)	9715	719.94
Quantize (T4)	925	86.82
Fir (T5)	2086	163.47
Dot_product (T6)	906	72.25
Convolution (T7)	871	65.84

Fig. 2 TPG for a practical system.

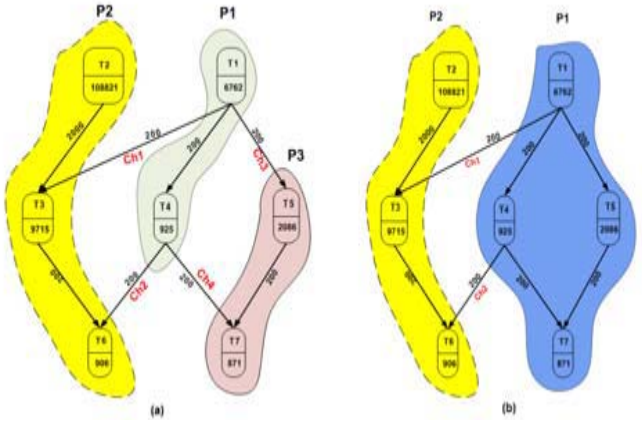


Fig. 3 Different architectures tasks mapping on (a) 3 cores, (b) 2 cores.

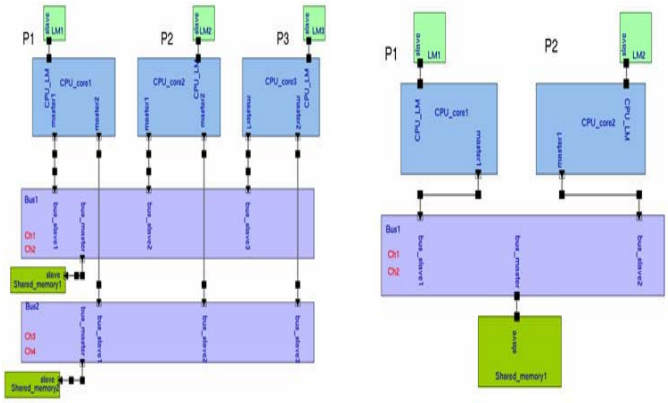


Fig. 4 TLM-based architecture. (a) 3-core, (b) 2-core.

For each architecture, simulation runs in AT mode which provides several orders of magnitude speedup over cycle accurate models while producing sufficiently accurate simulation results. For SystemC elaboration phase, LT (Loosely Timed) simulation mode, where no timing constraint is taken in account, is used for fast system bring-up. A clock speed of 100 MHz is used. The delay and power are ignored since they are negligible. The GANTT (scheduling chart) is plotted to illustrate the tasks execution schedule on the cores as

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shown in Figure 5. Different statistic information for various data transfers are determined to help the designer to compare power consumption and the resource idle time of different architectures as shown in Table I.

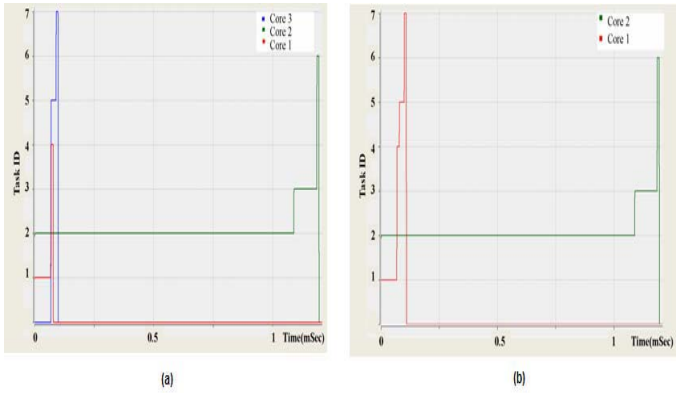

Fig. 5 GATT chart (a) 3-core, (b) 2-core.

Table 1: Comparing 2-cores and 3-cores architecture

Performance criterion		3-core	2-core
Power (mW)	**Dynamic**	1430	1059
	Clock	13	7
	Leakage	3	1
	Total power	1445	1067
Resource idle time (%)	**Processor cores**	63	64
	Busses	72	86

5. Conclusions

A new framework for TLM-based architecture exploration for multi-core system starting from TPG is presented. TLM provides fast and still accurate efficient exploration methodology Separating functionality, timing, and power aspects reduces the modeling effort and speeds exploring different architectures. The proposed approach not only contributes in dramatically decreasing the exploration time, but also eases design understanding, evaluation and analysis.

References.

[1] G. Martin. “Overview of the MPSoC Design Challenge,” in Proc. Of DAC’06, pp. 274-279, July 2006.
[2] F. Ghenassia, “Transaction-Level Modeling with SystemC: TLM Concepts and Applications for Embedded Systems,” Published by Springer, Netherlands, 2005.
[3] C. Silvano, W. Fornaciari, G. Palermo, V. Zaccaria, F. Castro, M. Martinez, R. Zafalon, S.Bocchio, M. Wouters, G. Vanmeerbeeck, P. Avasare, C. Couvreur, L. Onesti, C. Kavka, A. Turco, U. Bondi, G. Mariani, E. Villar, H. Posadas, C. Y. q. Wu, F. Dongrui, Z. Hao and T. Shibin. “MULTICUBE: Multi-objective design space exploration of multi-core architectures.” In IEEE Computer Society Annual Symposium on VLSI - ISVLSI, Kefalonia, Greece, July 2010.
[4] Hao Shen; Petrot, F.; , "MPSoC Communication Architecture Exploration Using an Abstraction Refinement Method," VLSI Design, 2008. VLSID 2008. 21st International Conference on , vol., no., pp.403-408, January 2008
[5] H. Youness, K. Sakanushi, Y. Takeuchi, A. Salem, A. Wahdan and M. Imai, “Optimal Scheme for Search State Space and Scheduling on Multiprocessor Systems”, IEICE Transaction On Fundamentals of Electronics, Communications and Computer Sciences, Vol. E92-A, No.4, pp.1088-1015, April 2009.
[6] Mentor Graphics® Vista Architect™ Tool [Online]: Available: http://www.mentor.com/products/esl/design_verification/vista_architect
[7] R. A. Bergamaschi, Y.W. Jiang,.”State systems-on-chip,” Design Automation Conference, pp. 638- 641, June 2003.

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Mohamed AbdElSalam received his B.Sc. and M.S Degree from Ain-Shams University, Cairo, Egypt, and Doctor of Information Science and Technology from Osaka University, Osaka, Japan. He joined Mentor Graphics 1998-2002 working in SW development of circuit simulation and IC layout tools, and development of ModuleWare library in FPGA Advantage/HDS tool, and again in 2008 to present, in Global R&D Egypt MED solutions as Technical lead, working on hardware emulation targets, Memory softmodels and Transaction/Virtual based Solutions. His research interest is in HW/SW co-design, System level design, and HW modeling of communication protocols IPs.

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