Low Power of Ring Oscillator Based on CNTFET

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Abstract

In this paper, architectures of NOT gate and conventional ring oscillator have been proposed using C-CNTFETs and their operational characteristics are checked using the simulator Agilent Design System (ADS). The CNTFETs use a semiconducting Carbon nanotube (CNT) channel controlled by isolated electrostatic gates. Circuit-compatible model of conventional CNTFET, which demonstrates n and p type switching behavior depending on the gate voltage, is implemented in ADS and the designs are extensively simulated in ADS. This paper introduces the analysis of the impact of diameter of CNT variations, especially logic switching propagation time and the oscillation time period.

The C-CNTFET inverter and ring oscillator are designed and their speeding and performances have investigated with the proposed compact mod el. In fact we have achieved for the ring oscillation RO6 an oscillation frequency equal to 7.04 GHz and power consumption equal to132.8 aW.

Keywords: *Carbon nanotube field effect transistors (CNTFET), Compact model, power consumption, Ring Oscillator.*

1. Introduction

In electronics and novel technological advances, transistors are the basic item. The nanostructures is used in the nanotransistors can be graphene, nanowires and nanotubes [1].

The first nanotransistor is developed in 1998 [1].

The carbon nanotube field effect transistors is indicated as CNTFETs have emerged as possible replaced for complementary metal-oxide-semiconductor is denoted as CMOS technology in terms of understanding of specific performance limits, identification of potential applications, physical modeling and superb electronic properties [2], [3], [4] and [5].

Indeed, CNTFETs are the most interesting structures for future nanoelectronics technology and are soon considered as favorable alternative for CMOS devices [6]. It's have near ballistic transport, exceptional characteristics, high accomplishment and low power consumption [6] and [7].

The power consumption has increase practically on Very-Large-Scale Integration is denoted as VLSI circuits with increase of number of transistors per unit chip area and rapidity.

The single walled nanotubes denoted as SWNTs are attractive for materials with unique properties, long lengths ranging from tens of nanometers to several centimeters, small diameters on the order of single digit nanometers, and thermal stabilities [8].

On the other hand, the increase in low power consumption inverter arises due to the fact that the CNTFETs is used a SWNTs as a channel.

The technology of CNT transistors is still emerged and the theory is still primitive [9] and [10]. The large numbers of models of CNTFETs have developed both theoretically and experimentally. In many analog and digital applications, CNTFETs are universal model of a nano device. Briefly the different types of CNTFETs compact models have demonstrated in literature we remind such as: the CNTFET model proposed by (Burke and al., 2002), CNTFET model proposed by (Raychowdhury and al., 2004), the high frequency CNTFET model proposed by (Bethoux et al., 2006), CNTFET model proposed by (Deng and al., 2007b), CNTFET model proposed by (Marulanda 2008), small-signal SWNT-FET device model proposed by (Amlani and al., 2009) and model for CNTFETs proposed by (Marani and al., 2011).

It is obvious that, mathematical and circuit model for metallic CNTs are investigate the speeding and performances design process.

The Stanford circuit-compatible compact model for the intrinsic channel region of the MOSFET-like SWNT-FETs is denoted as conventional CNTFETs (C-CNTFETs) [11].

The same model is enabled transient simulations of circuit as well as transfer (DC) characteristics.

The compact model is devised to allow an easy implementation in circuit simulators and is validated against numerical models in [9] and [12].

In nanoelectronic, the circuit of compact model is selected by reason the useful methods are developed the coefficients and equations used for the electrical design of the physical behaviour of a device. The term of compact is used to simplify these equations. On the other hand to criticize that analog and digital circuits are achieving the logic function correctly.

This model is appropriate to a range of carbon nanotube diameter is denoted as D_{CNT} between 1 to 3 nm. It aims at offering an improved physical approach of the D_{CNT} and the conduction band minima.

For this, it is necessary to accurate modeling of the impact of the device parameters and the including of both the new physical characteristics of the compact CNTFET models.

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In particular, the compact model is used when the device behaviour can be expressed as a set of equations non involving PDE. Thus it is possible to utilize some of the most useful tools available in electronic simulation software, having the graphic interface for the schematic drawing and the component libraries to obtain circuit equations automatically and the circuit netlist [13].
Nowadays, the CNTFET demonstrates the excellent performance Due to the small diameter, best source and drain metal contact and thin high-k gate insulator.
It is theoretically predicted that a short CNT operating in the quantum capacitance limit and the ballistic regime should be able to provide gain in the THz range [1].
This paper introduces the proposed resistance of the doped drain/source regions R_{DS} of involves the contribution to the compatible circuit model of the ballistic one-dimensional n- type of C-CNTFET proposed by [7]. We suggest the equations for estimating the parameters α_0, α_1 and α_2 of involve the contribution to the capacitors C_{GS} and C_{GD}.
In this work, the proposed model is implemented and is checked in ADS simulator. The ADS model is presented to simulate the C-CNTFET complementary inverter and C-CNTFET Ring Oscillator circuits with respect to expect the parameter variations. These circuits also exhibit low power consumption speed and performance. Besides the standard five-stage C-CNTFET ring oscillator is studied in this paper. It is a device which is realized by placing an odd number of the C-CNTFET complementary inverter (NOT gates) whose output V_{OUT} oscillates between two voltage levels, representing high (V_{DD}) and low (GND).
Finally this paper demonstrates that the conventional C-CNTFET, in combination with pass-gate logic, allows a very efficient implementation (NOT gate and the ring oscillator) having only few transistors, small delay and low power consumption.
The presentation of this paper is organized as follows. Section two gives a brief description of the mathematical and the circuit of C-CNTFET compact model. The ADS implementation of the I-V model is presented and the simulation results are displayed in section three. The conclusions are drawn in section four.

2. C-CNTFET Compact Model

A numerical model for ballistic conventional nano FETs is summarized in the computational procedure is given by [7], [8], [11], [12], [14], [15], [16], [17], [18] as below:

$$C_{Gi} = qN_0 \frac{AL}{K_B T} \exp(\xi_i), \quad for\ \xi_i \langle 0\ et\ V_{GS} \leq \Delta_1 \qquad (11)$$

- In the INESS model, V_{CNT} is considered as a continuous function (smooth factor: ε=5.10^{-4}) for the whole range of V_{GS}:

$$V_{CNT} = V_{GS} - 0.5\alpha(V_{GS} - \Delta_1) + 0.5\sqrt{[\alpha(V_{GS} - \Delta_1)]^2 + 4\varepsilon^2} \qquad (1)$$

Where the parameter α is given by:

$$\alpha = \alpha_0 + \alpha_1 V_{DS} + \alpha_2 V_{DS}^2 \qquad (2)$$

- The proposed parameters α_0, α_1 and α_2 are determined as indicated below [13]:

$$\alpha_0 = 0.7646 - 0.124 \times D_{CNT} + 0.018 \times D_{CNT}^2 \qquad (3)$$

$$\alpha_1 = -0.3206 + 0.181 \times D_{CNT} - 0.137 \times D_{CNT}^2 + 0.024 \times D_{CNT}^3 \qquad (4)$$

$$\alpha_2 = 0.107 - 0.137 \exp[-\frac{(D_{CNT} - 1.1075)}{0.9744}] \qquad (5)$$

- The drain current I_{DS} for the first subband is determined as:

$$I_D = \frac{4eK_B T}{h} \sum_{p=1}^{+\infty} [\ln(\frac{(1+\exp(-\xi_S))}{(1+\exp(-\xi_D))})] \qquad (6)$$

Where,

$$\xi_i = (\frac{V_{CNT} - \Delta_P - \mu_i}{K_B T}) \text{ for } i=_{S,D} \qquad (7)$$

- the conduction band minima for the first subband is obtained as below:

$$\Delta_1 = \frac{0.45}{D_{CNT}} \qquad (8)$$

Then the pth equilibrium conduction-band minima Δp is calculated by following equation:

$$\Delta_P = \Delta_1 \frac{(6p - 3 - (-1)^P)}{4} \qquad (9)$$

- For CNT with (n, m) chirality, the diameter of the zigzag nanotube (m=0), the D_{CNT} can be expressed as:

$$D_{CNT} = \frac{n\sqrt{3}.a_{C-C}}{\pi} = \frac{L_{CNT}}{\pi} \qquad (10)$$

Assume that a_{C-C} represents the inter-carbon-atom distance within the hexagonal lattice which is approximately 1.44 Å and the CNT length denoted as L_{CNT}.
- The capacitors C_{GS} and C_{GD}.

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$$C_{Gi} = qN_0 \frac{AL}{K_B T} \exp(\xi i)(1-\alpha), \quad (12)$$

$$for\ \xi i \langle 0\ et\ V_{GS} \geq \Delta_1$$

$$C_{Gi} = qN_0 \frac{BL}{K_B T}, \quad (13)$$

$$for\ \xi i \geq 0\ et\ V_{GS} \leq \Delta_1$$

$$C_{Gi} = qN_0 \frac{BL}{K_B T}(1-\alpha), \quad (14)$$

$$for\ \xi i \geq 0\ et\ v_{GS} \geq \Delta 1$$

$$N_0 = \frac{4K_B T}{3\pi V_\pi b} \quad (15)$$

$$A = -5.3\left(\Delta_1\right)^2 + 10\,\Delta_1 + 1 \quad (16)$$

$$B = 0.34\Delta_1 + 1 \quad (17)$$

- The CNTFET threshold voltage is given by:

$$V_{TH} = \frac{0.42}{D_{CNT}(nm)} \quad (18)$$

- The flat band voltage denoted as V_{FB} is determined as a function of CNT diameter as well:

$$V_{FB} = 0.143 + 1.104.\exp(-1.1965.D_{CNT}) \quad (19)$$

- The ultimate limit value of the transconductance gm can be expressed as:

$$g_m(\mu s) = \frac{4e^2}{h} = 1.6 \quad (20)$$

- The carrier mobility μ are calculated:

$$\mu = \frac{g_m.L_{CNT}^2}{C.V_{DS}} \quad (21)$$

- The gate oxide capacitance is computed from the well-known expression for a cylindrical structure where the nanotube is considered as equipotential:

$$C_{OX} = \frac{2\pi\varepsilon_{oxide}}{\ln(\frac{2t_{ox}}{D_{CNT}} + 1)} \quad (22)$$

The proposed model uses suitable approximations necessary for developing any circuit compatible compact model which presented in figure 1.

The voltage generator describes V_{FB} is the flat band voltage, R_D and R_S represent resistances of the doped drain and source regions, R_{DS} represents resistance of the doped drain/source regions, while C_{GS} and C_{GD} represent capacitances of gate-drain and gate-source, finally I_D represents drain current.

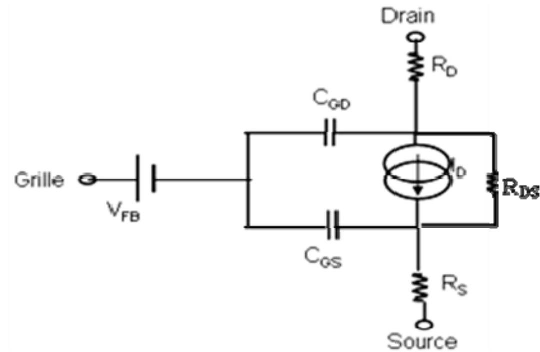

Fig. 1 The proposed ADS compatible circuit model of n- type of C-CNTFET.

In addition, unlike silicon-based MOS devices, in nanotransistor technology both n and p-type transistors have same carrier mobilities ($\mu_p = \mu_n$) with same current drive capabilities, which is very consequential for transistor sizing of the complex analog and digital circuits and same geometries [18].The typical C-CNTFET device is showing in figure 2.

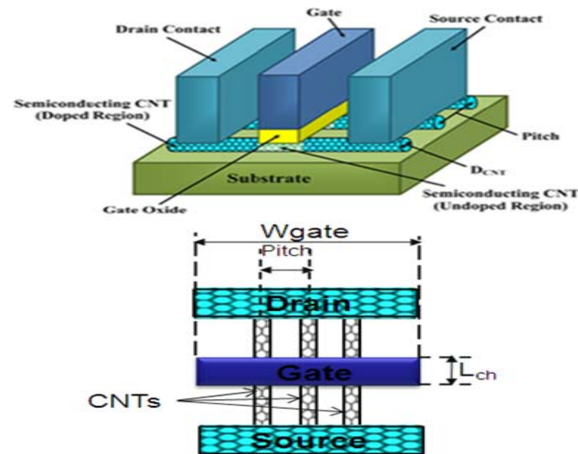

Fig. 2 The schematic of C-CNTFET.

The approximate width of the gate of a CNTFET can be calculated using the following equation [18]:

$$W = Min(W_{\min}, (N-1)Pitch + D_{CNT}) \quad (23)$$

Where N is the number of CNTs under the gate and W_{min} is the minimum width of the gate.

In order to verify the functionality of the digital circuits, we can determinate the values of the parameters of the equations 3, 4, 5, 8, 10, 18 and 19.

In fact we have fixed the value capacitances for V_{GS}=V_{DS}=0.5V, in the equations 11, 12, 13, 14, 15, 16 and

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17 to obtain an average values of C_{GD} and C_{GS} with thick HfO (t_{ox}=4nm) and high-k dielectric (ε_{ox}=16) [19].
We must use the important parameters of the C-CNTFET and their values, with brief descriptions listed in Table 1.

Table 1: Characterizes properties of C-CNTFETs

Parameters	*n- type of C-CNTFET*			*p- type of C-CNTFET*		
Chirality	(19,0)	(13,0)	(10,0)	(19,0)	(13,0)	(10,0)
D_{CNT} (nm)	1.487	1.018	0.783	1.487	1.018	0.783
L_{CNT} (nm)	4.66	3.19	2.45	4.66	3.19	2.45
Δ_1	0.28	0.41	0.53	0.28	0.41	0.53
α_0 (V)	0.62	0.65	0.67	0.62	0.65	0.67
α_1 (V^{-1})	-0.27	-0.25	-0.25	-0.27	-0.25	-0.25
α_2 (V^{-2})	0.01	-0.04	-0.08	0.01	-0.04	-0.08
V_{FB} (V)	0.32	0.46	0.57	-0.32	-0.46	-0.57
C_{GD} (aF)	41.97	27.90	21.69	81.65	58.13	46.36
C_{GS} (aF)	81.65	58.13	46.36	41.97	27.90	21.69
V_{TH}	0.289	0.428	0.559	-0.289	-0.428	-0.559
Gate length	32 (nm)					
Pitch	20 (nm)					

3. The C-CNTFETs circuits.

In our study, all parasitic capacitance or resistance of interconnects have been discarded. Yet, we include only included the inherent device characteristic with the fixed the values capacitance at room temperature (300 K).

3.1 Design of NOT Gate using C-CNTFET

The n-type CNTFETs is modeled and simulated in ADS and the (I–V) characteristics of n-type of C-CNTFETs are shown in figure 3 for the zigzag C-CNTFET featuring n=19, m=0. Figure 3 shows I_{DS}-V_{DS} characteristics for ten value V_{GS}.

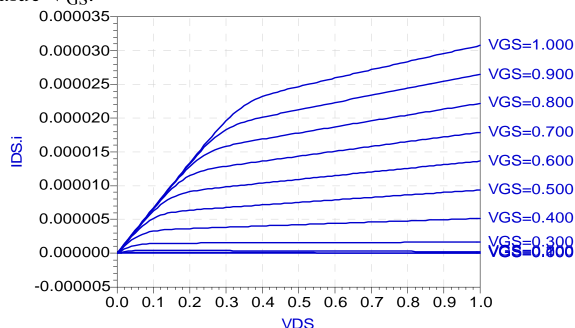

Fig3. Drain current versus source-drain bias of ADS compatible circuit model of n-type of C-CNTFET.

We have noted that it can be seen that I_{DS}=7.519µA for V_{DS}=V_{GS}=0.5V.
The C-CNTFET complementary inverter is simply formed by connecting both n and p-type C-CNTFET in series, with the latter inverted to operate from a single-voltage supply, as shown in figure 4.

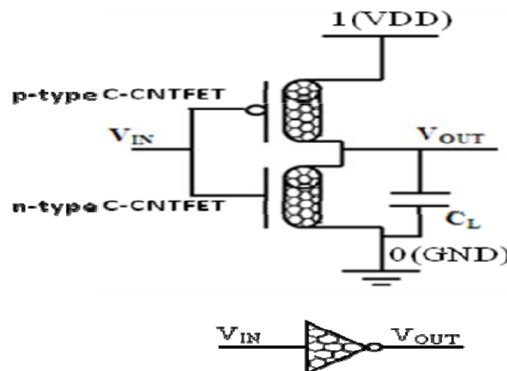

Fig4. C-CNTFET NOT Gate Circuit.

In this work both n-type and p-type CNTFETs are modeled and simulated in ADS that is used to predict the circuit behavior and to verify circuit designs.
The C-CNTFET complementary inverter (has the D_{CNT} equal to 1.487 nm for both n and p type) is simulated at different values of voltage power supply (0.5V, 1V, 1.5V and 2V). The voltage transfer characteristics is denoted as VTC of this circuit with a virtual 5 aF load is shown figure 5.

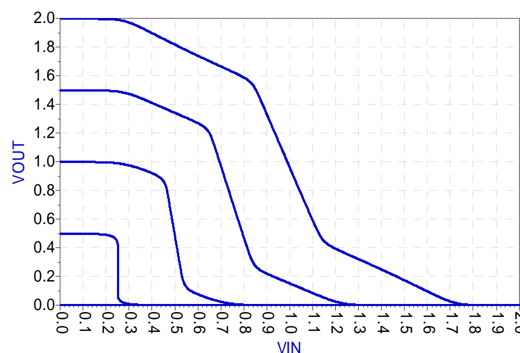

Fig5. The VTC of the 32nm C-CNTFET complementary inverter for different power supplies.

The following table presents the results obtained for the same circuit, in which we have showed the T_{PLH}, period T and T_{PLH}/T(%) ratio with different value of load capacitor C_L. The result of the transient simulation is summarized in table 2.
The simulated results show the fewer t_{PLH}/T(%) ratio is given from C_L equal to 5aF where t_{PLH} is delay time for V_{OUT} to change from low to high.

Table 2: Results of TPLH/T(%) for different value of CL.

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Load capacitor C_L (aF)	***Simulated results***		
	T(ps)	t_{PLH}(ps)	t_{PLH}/T(%)
1	59.8	1.07	1.78
2	59.8	1.16	1.93
3	60	1.25	2.08
4	60	1.36	2.26
5	60	1	1.66
50	59.8	7.85	13.12

The circuit shown in figure 4 is simulated for three D_{CNT} (1.487 nm, 1.018 nm and 0.783 nm) with a virtual 5 aF load.
The following table presents the results obtained for the same C-CNTFET complementary inverter, in which we show the T_{PLH}, T_{PHL}, delay and threshold voltage V_{TH} with different value of D_{CNT} for both n and p type of C-CNTFET.
The result of the transient simulation is summarized in table 3.
Where t_{PHL} is the delay time for output to change from high to low.

Table 3. Results of delay for a frequency equal to 16.66 Ghz and C_L=5aF.

D_{CNT} of C-CNTFET (nm)		***T_{PHL} (ps)***	***T_{PLH} (ps)***	***Delay (ps)***	***V_{TH} (mV)***
N-type	P-type				
1.487	1.487	0.54	0.53	0.535	0.13
1.018	1.018	0.94	0.93	0.935	0.18
0.783	0.783	2.3	2.3	2.3	0.19
1.487	1.018	0.94	0.52	0.73	0.10
1.487	0.783	2.7	0.52	1.61	0.06
1.018	0.783	2.7	0.92	1.81	0.13
1.018	1.487	0.52	0.92	0.72	0.22
0.783	1.487	0.52	2.7	1.61	0.29
0.783	1.018	0.94	2.7	1.82	0.24

We conclude that the complementary inverter which has the D_{CNT} (equal to 1.487 nm for both n-type and p-type of C-CNTFET) is faster than the other diameter of CNT.
We have noted that the D_{CNT} decease the V_{TH} increase for a NOT gate.
We use voltage power supply 500 mV and the C-CNTFET of D_{CNT} equal to 1.487 nm for both n and p type and having the parameters values as shown in table1 with load capacitance C_L equal to 5 aF.
The simulated output voltage of C-CNTFET complementary inverter is shown in Figure 6 and Figure 7.
As shown in figure 6, we observe that the waveforms corresponding to the input V_{IN} is observed to be automatically the inverse of output signal V_{OUT}.
Also, we observe that the switching threshold is ideal for C-CNTFET complementary inverter which has D_{CNT} is equal to1.42 nm for the n and p with a high noise margin as shown in figure 7.

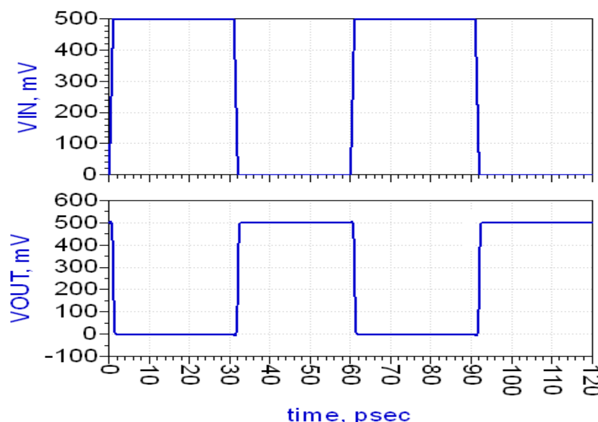

Fig 6. C-CNTFET NOT Gate input/output.

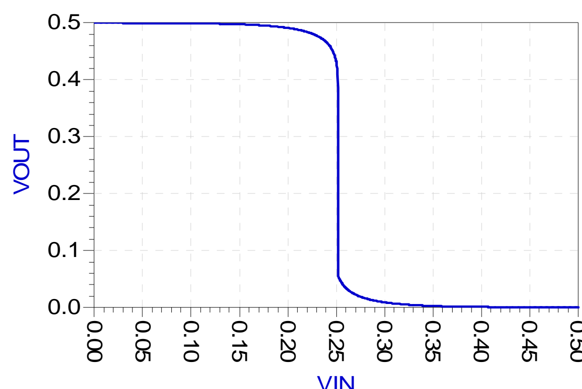

Fig 7. Transfer characteristics of the C-CNTFET complementary inverter output.

Table 4. Compared results with recent C-CNTFETs inverter research.

References	***Delay***	***Power (µW)***	***PDP (a J)***
[This work]	0.53(ps)	0.24	0.12
[20]	2.42(ps)	0.11	0.26
[13]	2.52(ns)	18	45.3

The performance summary and the comparison of this work to previously reported performance which used the same technology (32nm) are listed in table 4.
Table 4 compares the simulated results of this work to some recently reported NOT gate in nanotransistor C-CNTFETs.
We note that the NOT gate gives a low power-delay product (PDP), power consumption and faster delay comparing to the NOT gates are presented in these references.

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3.1 DESIGN OF RING OSCILLATOR USING C-CNTFET

A ring oscillator is a circuit which is realized by placing an odd number of the C-CNTFETs complementary inverter (NOT gates) whose output V_{OUT} oscillates between two voltage levels, representing low (GND) and high (V_{DD}) .
A design circuit of a simple five C-CNTFETs complementary inverter ring oscillator with the V_{OUT} of the last stage fed back to the V_{IN} of the first stage is shown in figure 8.

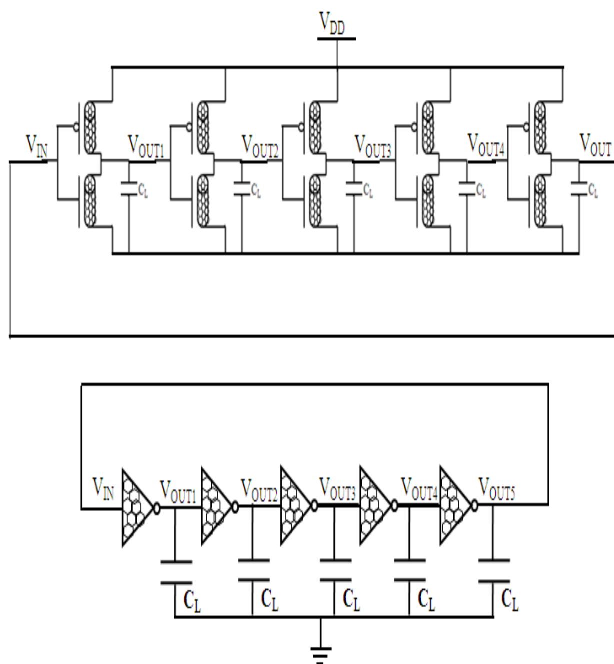

Fig 8. C-CNTFET ring oscillator for 5 stage.

The C-CNTFET Ring oscillator is the privileged choice to generate a square signal for frequency range of THz.
The behavior of this circuit is as follows, it will oscillate and for each half-period, the signal will propagate around the loop with an inversion. This change will propagate through all five C-CNTFETs complementary inverters in a time of T/2, at which time the V_{OUT} of the first inverter must switch to a 0V and after an additional time of T/2 switching the V_{OUT} of the first inverter back to a 0.5V.
Assuming each inverter in the oscillator is used as a delay of τ_p and that there are five C-CNTFET complementary inverter [21].

$$\frac{T}{2} = N\tau_p \qquad (24)$$

Where N is the number of delay stages and τ_p is the delay time of each stage in the ring oscillator.
The frequency is the reciprocal of the period, resulting in the frequency of oscillation is shown in the following equation:

$$f_{osc} = \frac{1}{2N\tau_p} = \frac{g_m}{2NC_L} \qquad (25)$$

Where, C_L is the load capacitance of delay stage without parasitic elements.
The ring oscillator is denoted as RO is simulated at different values of D_{CNT} and C_L.
We present the simulated results of six different sizes of D_{CNT} of C-CNTFET ring oscillator:

- RO1 is the RO which is used the C-CNTFET complementary inverter (has the D_{CNT} equal to 0.783 nm for both n and p type).
- RO2 is the RO is used the C-CNTFET complementary inverter (has the D_{CNT} equal to 1.018 nm for both n and p type).
- RO3 is the RO which is used the C-CNTFET complementary inverter (has the D_{CNT} equal to 1.487 nm for both n and p type).
- RO4 is the RO which is used the C-CNTFET complementary inverter (has the D_{CNT} equal to 0.783 nm for n- type and has the D_{CNT} equal to 1.018 nm for p- type).
- RO5 is the RO which is used the C-CNTFET complementary inverter (has the D_{CNT} equal to 1.018 nm for n- type and has the D_{CNT} equal to 1.487 nm for p- type).
- RO6 is the RO which is used the C-CNTFET complementary inverter (has the D_{CNT} equal to 0.783 nm for n- type and has the D_{CNT} equal to 1.487 nm for p- type).

The following table presents the results obtained for the circuit shown in figure 8, in which we have showed the T_{PLH}, period T, T_{PLH}/T(%) ratio and power for RO1, RO2, RO3, RO4, RO5 and RO6. The result of the transient simulation is summarized in table 5.
Simulation results show that the fewer t_{PLH}/T (%) ratio equal to 5.25 (%) is for RO6 which is carried for C_L equal to 0.5 aF.
We have observed that the analysis of the impact of diameter of CNT variations, especially in term delay, the oscillation frequency.
We note the variation of load capacitor C_L has no effect in term power consumption.

Table 5. Summarized results

	C_L	t_{PLH}	T_{osc}	t_{PLH}/T_{osc} (%)	*Power*
	5(pF)	4.06µs	29.2µs	13.90	59.25

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RO1	0.5(pF)	384.4ns	2.9µs	13.25	(aW)
	0.05(pF)	39.4ns	290ns	13.58	
	5(fF)	4.07ps	29.2ps	13.93	
	0.5(fF)	430.6ps	2.92ns	14.74	
	0.05(fF)	40.01ps	46.6ps	12.42	
	0.005(fF)	6.016ps	46.6ps	12.90	
RO2	5(pF)	1.189µs	7.8µs	15.24	0.28 (pW)
	0.5(pF)	139.4ns	780ns	17.87	
	0.05(pF)	12.01ns	78ns	15.39	
	5(fF)	1.201ns	7.8ns	15.39	
	0.5(fF)	117.6ps	780ps	15.07	
	0.05(fF)	13.11ps	83ps	15.79	
	0.005(fF)	2.816ps	13.1ps	21.49	
RO3	5(pF)	801.1ns	3µs	26.7	75.83 (aW)
	0.5(pF)	87.11ns	300ns	29.03	
	0.05(pF)	8.611ns	30ns	28.7	
	5(fF)	925ps	3ns	30.83	
	0.5(fF)	80.33ps	300ps	26.71	
	0.05(fF)	8.63ps	32.8ps	26.32	
	0.005(fF)	1.34ps	6ps	22.31	
RO4	5(pF)	1.23µs	17.8µs	6.94	7.72 (aW)
	0.5(pF)	131.1ns	1.78µs	7.32	
	0.05(pF)	14.11ns	178ns	7.92	
	5(fF)	1.5ns	17.8ns	8.42	
	0.5(fF)	distorted signal			
	0.05(fF)				
	0.005(fF)				
RO5	5(pF)	0.70µs	5.1µs	13.80	0.35 (pW)
	0.5(pF)	62.66ns	510ns	12.28	
	0.05(pF)	6.26ns	51ns	12.27	
	5(fF)	675.1ps	5.1ns	13.23	
	0.5(fF)	67.51ps	510ps	13.23	
	0.05(fF)	7.191ps	53.8ps	13.36	
	0.005(fF)	2.326ps	8.75ps	26.58	
RO6	5(pF)	0.71µs	13.3µs	5.39	132.8 (aW)
	0.5(pF)	77.61ns	1.33µs	5.83	
	0.05(pF)	7.11ns	133.2ns	5.33	
	5(fF)	761ps	13.32ns	5.71	
	0.5(fF)	71.1ps	1.34ns	5.30	
	0.05(fF)	7.46ps	142ps	5.25	
	0.005(fF)	1.071ps	20ps	5.35	

We conclude that the RO6 has the fewer $t_{PLH}/T(\%)$ ratio than the other ROs.
In order to, we observe that the transient behavior of the output V_{OUT} RO6 circuit generates the best square signal.
Figure 9 shows the result of the transient simulation of RO6 with C_L equal to 0.5 aF. The output spectrum of RO6 is shown in figure 10 where the center frequency is 7 GHz and presents the 14.25 dBm.

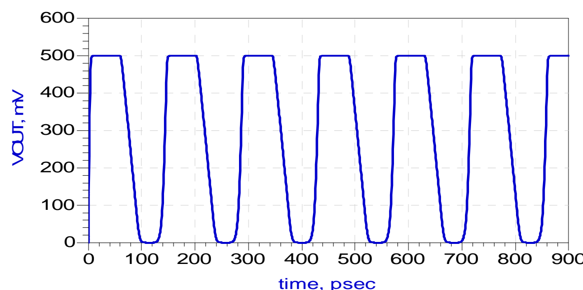

Fig9. Transient characteristic of C-CNTFET RO6.

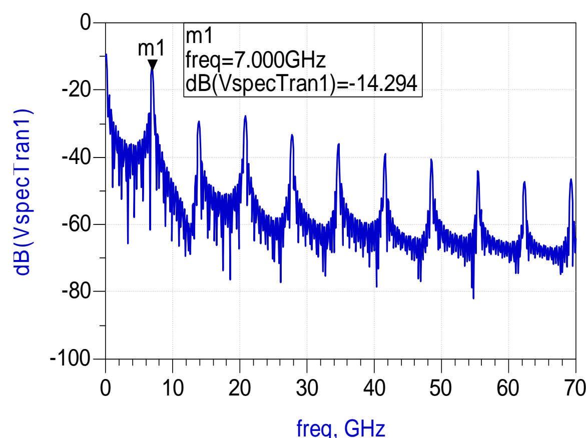

Fig.10. Output spectrum of the RO6.

We note that power of the RO3 is equal to 75.83 aW for I_{OUT} equal to 841.6 fA. But the power of the RO6 is equal to 132.8 aW for I_{OUT} equal to 595.2 fA.

The results which summarized in table 5, it is clear that the RO4 has the lowest power consumption equal to 7.72 aW. The oscillation frequency of the RO3, RO4 and RO6 are 166.66 GHz, 56 KHz and 7.04 GHz, respectively.
The RO6 presents a low $t_{PLH}/T(\%)$ ratio comparing to the ROs illustrated in this table, the RO3 presents the highest oscillation frequency and the RO4 presents the lowest power consumption.
Thus, these results are a compromise between the oscillation frequency and the power consumption. The ring oscillators the RO6 considerate the best choice.

4. Conclusion

In this paper, the proposed compact model shown in figure1 is implemented to examine the behavior of a C-CNTFET which is used at different CNT diameters. In particular the importance of C_{GD}, C_{GS}, V_{FB} and C_L have been demonstrated.
The techniques used in our proposed design along with exploiting the relationship between V_{TH} and D_{CNT}, have made it an efficient design which uses a minimum number of transistors. Moreover, the proposed model of C-

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CNTFET complementary inverter and C-CNTFET ring oscillator circuits have been employed. The results in analytic form and in simulation using ADS have been presented.
This proposed model is firstly used to devise the design of C-CNTFET complementary inverter circuit and the simulations are validated in terms of delay, power consumption, and PDP.
The simulated results show the excellent power and delay for the C-CNTFETs which has D_{CNT} equal to 1.487 nm for both n and p type.
On the other hand, is used to devise the design of C-CNTFET ring oscillator circuit and the performances are studied in terms of the frequency of oscillation, the output spectrum and power consumption. The analysis of the impact of diameter of CNT variations, especially delay, the oscillation frequency and the power consumption have been demonstrated in this work.
The output characteristics confirm that our digital circuits are achieving the logic function correctly.
The results obtained from the simulations prove that CNT is far superior to silicon as a semiconducting material.

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