One Method for Via Equivalent Circuit Extraction Based on Structural Segmentation

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Abstract

As the signal frequency increases, the accurate and fast modeling for vias structure in multi-layer substrate is very important to performance analysis of high speed circuit. According to the skin effect and RL ladder circuit model, the equivalent circuit of via base on structural segmentation is presented in this paper. Vias structure is decomposed into some segmented sub-structure based on the routing layer. The equivalent circuit of each substructure is modeled on the basis of RL ladder circuit and numerical calculation method. And then, a complete equivalent circuit of the entire vias structure is modeled. Meanwhile, the equivalent circuit model of two adjacent via structure is established with coupling capacitance and coupled inductor. Finally, the simulation results of the equivalent circuit model in this paper are agreed to the results gained from HFSS within 8GHZ.

Key words: Vias, Equivalent circuit, Ladder circuit, Structural segmentation

1. Introduction

With the increase of the signal frequency and circuit speed, the effects of vias on circuit performance are more important. Being the discontinuity of the vias structure in transmission path, partial incident waves will reflect at the end point and the reflected waves will return to the source point. There become parallel planar waveguide between source and ground level when the current flow through the vertical vias. It will cause serious impact (such as the issues of signal integrity and power integrity) on the signal transmission. So, modeling the accurate and fast equivalent circuit model based on vias structure is very important to performance analysis in high speed circuit.

Recently, modeling and analysis method of vias mainly includes two kinds of aspects: analysis of circuit simulation and analysis of electromagnetic simulation. The via hole can be modeled as a cascade of capacitances and inductances, the values of the capacitances can be computed by FASTCAP, and the inductance values can be obtained by a closed form formula^[1]. full-wave modeling of vertical vias in multilayered circuits was presented in^[2],in which the analysis of the interior problem was based upon the cylindrical wave expansion of the magnetic field Green's function, and the exterior problem of the via and the transmission line was analyzed using the method of moments approach. Some other analysis methods, such as Finite Difference Time Domain (FDTD)^[3], Method of Moments (MOM)^[4] and Partial Element Equivalent Circuit (PEEC)^[5] were also used in the analysis of vias.

Many scholars have been proposed that via structure can be equivalent as a π -type network with one capacitance and one inductor^[6]. However, because of ignoring the influence of skin effect and interaction of different layers, the π -type network method could not accurately describe the vias structure in multi-layer board. As the signal frequency increases, the traditional lumped circuit and distributed RLC are no longer appropriate for vias structure due to skin effect and adjacent coupling effect. On the basis of the influence of frequency change on equivalent circuit, this paper proposes a new equivalent circuit model for vias structure. By compared with three-



dimensional full-wave simulation, the equivalent circuit model of vias structure has good similarity within 8 GHZ.

2. Extraction of equivalent circuit for via structure

2.1 The frequency-dependent equivalent circuit model

With the increases of signal frequency, the skin effect of transmission line is more and more important, therefore the equivalent circuit parameters of transmission line have obvious frequency-dependent characters in highcircuit system^[7]. The three-dimensional frequency electromagnetic field analysis has high accuracy in calculating the inductance and inductance frequencydependent distribution parameter, but because the partial inductance matrix is dense matrix and R(f), L(f) are the correlation function of frequency, so the calculation precision is lower and the calculation time is longer. An improved RL ladder circuit model proposed is adopted in this paper to describe the skin effect of vias structure, in which only four RL ladder circuit can accurately describe the skin effect of vias structure, the circuit model of ^[8] is shown in figure 1.



Figure 1. RL network instead of the frequency-dependent circuit

The improved RL ladder circuit employed in this paper is composed by four resistors and four inductors (R1-R4, L0-L3). The DC resistor R1 and low frequency inductor L0 of via structure can be obtained using the method in ^[9].Ri and Li can be gained using the method in ^[8]. Thus, instead of frequency-dependent equivalent circuit model of via structure, the ladder circuit can be well applied without a great number of numerical calculations, only needs to know the construction dimension and the material property.

2.2 The exaction of equivalent circuit for via structure

Via structure is used to connect transmission of different layers in multi-layer boards. Impedance mismatch will be caused in transmission path and induce signal integrity problem. When the signal frequency is less than 10GHz, the dimension of via structure is much less than one eighth of wavelength, so the effects on the interaction of electric and magnetic fields of via structure can be negligible according to law of experience. The capacitors and inductors of via structure can be calculated, and the influences of crosstalk between two adjacent vias can be approximately described as capacitive coupling and inductive coupling^[10]. In this paper, the wiring layers of substrate are decided as ideal plane, and the interaction of structure in different layers can be ignored. The RL ladder circuit mentioned above is employed to replace the frequency-dependent equivalent circuit parameters in order to accurately describe via structure using equivalent circuit. Therefore, only capacitors, DC resistors and inductors in low frequency are needed to calculate.

The extraction method of equivalent circuit for via structure proposed in this paper is to first decompose via structure in substrate with N-layer wiring layer (including top and bottom layer) into N-1 parts, that is, a separate structure is between adjacent layers. And then obtain the equivalent circuit contains RL ladder circuit for separate structure, respectively. Finally, connect the separate structures of equivalent circuit into an entirety. To analyze the influence of crosstalk between two adjacent vias, first of all, figure out the coupling capacitors and inductors of the adjacent via structure between layers, which can be used to connect two parts of via equivalent circuit so as to get the complete equivalent circuit model of double vias structure. The simple double vias model is shown in Figure 2.

With via runs through the four-layer substrate as an example, this paper divides via structure into three parts: the top layer, middle portion and bottom layer ^[11]. The equivalent capacitor of each part of structure is composed of the relative capacitor between via and each ground plane, all connected in parallel. Figure 2 shows the equivalent capacitor of top structure. The capacitors caused by top layer can be divided into C1, C2 and C3, where C1 is the capacitor between the pad of top layer and ground plane (including N1 and N2 plane), C2 is the capacitor between via and N1 ground plane, C2 is the capacitor between via and N2 ground plane.



Figure 2. Double vias model and capacitor of the top structure



Each ground plane can be approximately considered as no effects on magnetic field when the signal frequency is less than 10GHz. The DC inductor of RL network and coupling inductor of double via structure can be obtained by using the method below^[9].

$$L_{pf_{ij}} = \int_{bi}^{ci} \int_{bj}^{cj} \frac{dl_i \cdot dl_j}{r_{ij}}$$
(1)

$$L_{p_{km}} = \lim_{\substack{K \to \infty \\ M \to \infty}} = \frac{1}{KM} \sum_{i=1}^{K} \sum_{j=1}^{M} L_{pf_{ij}}$$
(2)

Where, Lpfij is mutual inductor of partial components, Lpkm is the mutual inductor of via structure.

In via structure, to accurately extract the capacitors between via structure and ground plane or vias need complex mathematical calculation. This paper adopts a model reduction method to extract the capacitors of structure. As the structure shown in Figure 3, a DC voltage source is added between two conductors in order to acquire the capacitor between the conductor structure and ground plane.



Figure 3. Extraction for equivalent capacitor of via structure

The capacitor of partial structure can be gained by the expression below ^[12].

$$C_{p} = \frac{Q}{V_{0}}$$
(3)

Where,

$$Q = \int_{r_1}^{h} \frac{4\pi\varepsilon V_0 r}{2(r_1 - r_0) + \pi (r - r_1)} dr$$
(4)

Therefore,

$$C_{p} = \frac{4\varepsilon}{\pi} \ln[2(r_{1} - r_{0}) + \pi(h - r_{1})]^{2(r_{0} - r_{1})} + 4\varepsilon(h - r_{1}) + \frac{4\varepsilon}{\pi} \ln[2(r_{1} - r_{0}) + \pi(h - r_{1})]^{zr_{1}} - \frac{4\varepsilon}{\pi} \ln[2(r_{1} - r_{0}) + \pi(h - r_{1})]^{zr_{1}} + \frac{4\varepsilon}{\pi} \ln[2(r_{1} - r_{0}) + \pi(h - r_{1})]^{zr_{1}} + \frac{4\varepsilon}{\pi} \ln[2(r_{1} - r_{0}) + \pi(h - r_{1})]^{zr_{1}} + \frac{4\varepsilon}{\pi} \ln[2(r_{1} - r_{0}) + \pi(h - r_{1})]^{zr_{1}} + \frac{4\varepsilon}{\pi} \ln[2(r_{1} - r_{0}) + \pi(h - r_{1})]^{zr_{1}} + \frac{4\varepsilon}{\pi} \ln[2(r_{1} - r_{0}) + \pi(h - r_{1})]^{zr_{1}} + \frac{4\varepsilon}{\pi} \ln[2(r_{1} - r_{0}) + \pi(h - r_{1})]^{zr_{1}} + \frac{4\varepsilon}{\pi} \ln[2(r_{1} - r_{0}) + \pi(h - r_{1})]^{zr_{1}} + \frac{4\varepsilon}{\pi} \ln[2(r_{1} - r_{0}) + \pi(h - r_{1})]^{zr_{1}} + \frac{4\varepsilon}{\pi} \ln[2(r_{1} - r_{0}) + \pi(h - r_{1})]^{zr_{1}} + \frac{4\varepsilon}{\pi} \ln[2(r_{1} - r_{0}) + \pi(h - r_{1})]^{zr_{1}} + \frac{4\varepsilon}{\pi} \ln[2(r_{1} - r_{0}) + \pi(h - r_{1})]^{zr_{1}} + \frac{4\varepsilon}{\pi} \ln[2(r_{1} - r_{0}) + \pi(h - r_{1})]^{zr_{1}} + \frac{4\varepsilon}{\pi} \ln[2(r_{1} - r_{0}) + \pi(h - r_{1})]^{zr_{1}} + \frac{4\varepsilon}{\pi} \ln[2(r_{1} - r_{0}) + \pi(h - r_{1})]^{zr_{1}} + \frac{4\varepsilon}{\pi} \ln[2(r_{1} - r_{0}) + \pi(h - r_{1})]^{zr_{1}} + \frac{4\varepsilon}{\pi} \ln[2(r_{1} - r_{0}) + \pi(h - r_{1})]^{zr_{1}} + \frac{4\varepsilon}{\pi} \ln[2(r_{1} - r_{0}) + \pi(h - r_{1})]^{zr_{1}} + \frac{4\varepsilon}{\pi} \ln[2(r_{1} - r_{0}) + \pi(h - r_{1})]^{zr_{1}} + \frac{4\varepsilon}{\pi} \ln[2(r_{1} - r_{0}) + \pi(h - r_{1})]^{zr_{1}} + \frac{4\varepsilon}{\pi} \ln[2(r_{1} - r_{0}) + \pi(h - r_{1})]^{zr_{1}} + \frac{4\varepsilon}{\pi} \ln[2(r_{1} - r_{0}) + \pi(h - r_{1})]^{zr_{1}} + \frac{4\varepsilon}{\pi} \ln[2(r_{1} - r_{0}) + \pi(h - r_{1})]^{zr_{1}} + \frac{4\varepsilon}{\pi} \ln[2(r_{1} - r_{0}) + \pi(h - r_{1})]^{zr_{1}} + \frac{4\varepsilon}{\pi} \ln[2(r_{1} - r_{0}) + \pi(h - r_{1})]^{zr_{1}} + \frac{4\varepsilon}{\pi} \ln[2(r_{1} - r_{0}) + \pi(h - r_{1})]^{zr_{1}} + \frac{4\varepsilon}{\pi} \ln[2(r_{1} - r_{0}) + \pi(h - r_{1})]^{zr_{1}} + \frac{4\varepsilon}{\pi} \ln[2(r_{1} - r_{0}) + \pi(h - r_{1})]^{zr_{1}} + \frac{4\varepsilon}{\pi} \ln[2(r_{1} - r_{0}) + \pi(h - r_{0}) + \pi(h - r_{1})]^{zr_{1}} + \frac{4\varepsilon}{\pi} \ln[2(r_{1} - r_{0}) + \pi(h - r_{1})]^{zr_{1}} + \frac{4\varepsilon}{\pi} \ln[2(r_{1} - r_{0}) + \pi(h - r_{1})]^{zr_{1}} + \frac{4\varepsilon}{\pi} \ln[2(r_{1} - r_{0}) + \pi(h - r_{1})]^{zr_{1}} + \frac{4\varepsilon}{\pi} \ln[2(r_{1} - r_{0}) + \pi(h - r_{1})]^{zr_{1}} + \frac{4\varepsilon}{\pi} \ln[2(r_{1} - r_{0}) + \pi(h - r_{0})]^{zr_{1}} + \frac{4\varepsilon}{\pi} \ln[2(r_$$

Where, Cp is the capacitor of via structure, r1 is the radius of anti-pad, r0 is the radius of via, h is the height between via and ground plane.



(a) Model of single via



(b) Model of double vias

Figure 4. Equivalent circuit of the top structure

Based on the calculation method mentioned above, the equivalent circuit model for the top structure of single via and double vias are shown as Figure 4. Similarly, the equivalent circuit model for middle and bottom structure can be got, and the equivalent circuit model of double vias can be obtained through series method as shown in Figure 5.



Figure 5. Equivalent circuit model of double vias structure

3. Verification of model

In order to validate the accuracy of equivalent circuit model proposed by this paper, a double vias model is given as Figure 1. The material of substrate is FR4, the dielectric constant is 4.2, the dielectric loss tangent is 0.015, the thickness between pad and ground plane is 0.03mm, the diameters of via structure, pad and anti-pad are 0.23mm, 0.38mm and 0.68mm respectively, the distance between vias is 1.3mm, the distance between top and bottom layer of substrate is 0.75mm, and the distance between middle parts is 1mm.

The comparison of S parameters obtained by equivalent circuit model(using ADS software) and three-dimensional full-wave simulation(using Ansoft HFSS software) is shown in Figure 6, in which,S11 is return loss of via



structure, S21 is transmission loss. Similarly, the S parameters of double vias structure obtained by equivalent circuit model and three-dimensional full-wave simulation is shown in Figure 7, in which, S13 is near-end crosstalk, S14 is far-end crosstalk.



Figure 6. Return loss of single via

Table 1:Comparison of S11(dB) and the errors with HFSS

Frequency	HFSS	Method	This	Errors
(GHz)	Simulation	of [6]	paper	
2	-21.61	-24.42	-21.91	1.18%
4	-16.16	-18.48	-15.95	1.29%
6	-12.93	-15.09	-12.74	1.47%
8	-11.15	-12.78	-10.66	4.39%
9	-10.97	-11.37	-9.86	10.11%
10	-10 71	-10.08	-9.28	13 53%



Figure 7. Coupling parameters of double vias structure

Table 2: Comparison of S13(dB) and the errors with HFSS

Frequency	HFSS	This	Errors
(GHz)	Simulation	paper	
2	-34.04	-34.13	0.26%
4	-26.71	-26.84	0.48%
6	-21.81	-21.95	0.64%
8	-18.66	-18.20	2.46%
9	-18.33	-16.60	9.43%
10	-18.10	-15.15	16.2%

From Figure 6 and Table 1, we know that the return loss obtained by the method proposed in this paper and the results gained from HFSS are well similar with the error less than 5% within 8GHz. When the frequency is more

than 8GHz, the error increases to more than 10%. The reason is that the wavelength of substrate is less than 30mm, which is no longer quite long when the frequency is upper 8GHz,. Therefore, the equivalent circuit model can' t well describe via model. The Table 1 indicates that the results obtained from the method in this paper are close to the results gained from full wave analysis, compared with the method in ^[6]. The Figure 7 and Table 2 shows that the analysis of crosstalk between double vias structure obtained by the method proposed in this paper and the results gained from HFSS are well similar with the error less than 2.5% within 8GHz. So, the method proposed in this paper can accurately describe the transmission characteristic of via structure, and for the double vias structure, can precisely describe the crosstalk between vias.

4. Conclusions

Along with the increasing digital signal frequency, the influences of via structure on signal transmission get more and more attention. The effects between adjacent vias can' t be ignored besides the influences of pad and antipad on via signal transmission. This paper proposed a new extraction method for via equivalent circuit. On the basis of wiring layers of multi-layer substrate, this method divides via into several separated structures, the equivalent circuit model of which are cascaded to get the equivalent circuit model of via structure. Meanwhile, the equivalent circuit model of adjacent double vias structure is established according to the coupling capacitor and inductor between vias. This paper proposed a method that using the improved RL ladder circuit mode instead of frequency-dependent inductors and resistors, considering the influences of skin effect on via equivalent circuit model. This method improves the precision of model and reduces the complexity of calculation. The simulation results of analyzing the equivalent circuit model obtained from the method proposed in this paper and the results gained from HFSS are well similar. In this paper, the influences of adjacent effects between vias on coupling inductors are neglected, and the method is only suitable within 8GHz.

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