Development of Receiver Stimulator for Auditory Prosthesis

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Abstract

T***he Auditory Prosthesis (AP) is an electronic device that can provide hearing sensations to people who are profoundly deaf by stimulating the auditory nerve via an array of electrodes with an electric current allowing them to understand the speech. The AP system consists of two hardware functional units such as Body Worn Speech Processor (BWSP) and Receiver Stimulator. The prototype model of Receiver Stimulator for Auditory Prosthesis (RSAP) consists of Speech Data Decoder, DAC, ADC, constant current generator, electrode selection logic, switch matrix and simulated electrode resistance array. The laboratory model of speech processor is designed to implement the Continuous Interleaved Sampling (CIS) speech processing algorithm which generates the information required for electrode stimulation based on the speech / audio data. Speech Data Decoder receives the encoded speech data via an inductive RF transcutaneous link from speech processor. Twelve channels of auditory Prosthesis with selectable eight electrodes for stimulation of simulated electrode resistance array are used for testing. The RSAP is validated by using the test data generated by the laboratory prototype of speech processor. The experimental results are obtained from specific speech/sound tests using a high-speed data acquisition system and found satisfactory.***

Keywords: *Receiver-stimulator, auditory prosthesis, microcontroller, Transcutaneous RF link.*

1. Introduction

The cochlear implant or Auditory Prosthesis (AP) has recently emerged as clinically acceptable prosthesis for aiding people suffering from a profound to total sensorineural hearing loss [1]. Several types of electronic hearing prostheses are now in widespread use by large number of people around the world. Today high performance and highly reliable multi channel auditory Prosthesis are available from various vendors such as Nucleus, Clarion, and Med-El etc [1]. These devices are expensive and not affordable by developing countries like India, China, Pakistan etc. [2-3]. Our aim is to design and develop low cost, high performance and highly reliable Auditory Prosthesis for use in developing countries. The developed system comprises the following main components: Body-Worn Speech Processor, a transcutaneous RF link, the prototype model of a 12 channel Receiver Stimulator for Auditory Prosthesis, and an array of electrodes.

The laboratory model of BWSP is a programmable speech processor [4-5] that implements 4 to 8 channels CIS algorithm [6-7] based on the number of active electrodes. The selection of active electrodes of each patient is determined by using the Clinical Programming Software (CPS) [8]. It can implement 4/5/6/7/8 CIS algorithm in which the frequency band of 200-6600Hz is logarithmically distributed to 4/5/6/7/8 bands/channels and set the patient specific compression values such as threshold and most comfort levels. It encodes the processed speech/sound information protocol specified in BWSP. The encoded speech data with Amplitude Shift Key (ASK) modulation is transmitted via radio-frequency (RF) transmitter, which is coupled to the Auditory Prosthesis via a transcutaneous inductive link. The ASK demodulator [9-11] in the prototype RSAP demodulates the incoming RF signal and reconstructs the encoded speech data. The encoded speech data is decoded by Speech Data Decoder and delivers electric current pulses with specified parameters to the selected channel in the electrode array.

The design as well as development of the prototype model of a 12 channel Receiver stimulator for Auditory Prosthesis is addressed in the present paper, covering both the Hardware and Software parts. The Hardware part covers the design and implementation of Speech data Decoder and Microcontroller interfacing between various analog and digital circuitry. The software part covers the embedded programs written for implementation of Speech data stimulation and impedance telemetry that sends back to speech processor the encoded electrode impedance data of each channel via RF transcutaneous inductive link.. It also covers the protocol implementation for Speech data stimulation from the data generated by the speech encoder in BWSP and the protocol used in the impedance telemetry for identifying the patient specific active electrode contacts.

features of DS89c420 are used for real-time speech processing by the BWSP. Speech Decoder performs two essential functions such as Speech Processing and Impedance Telemetry. At any instant of time, Speech Data

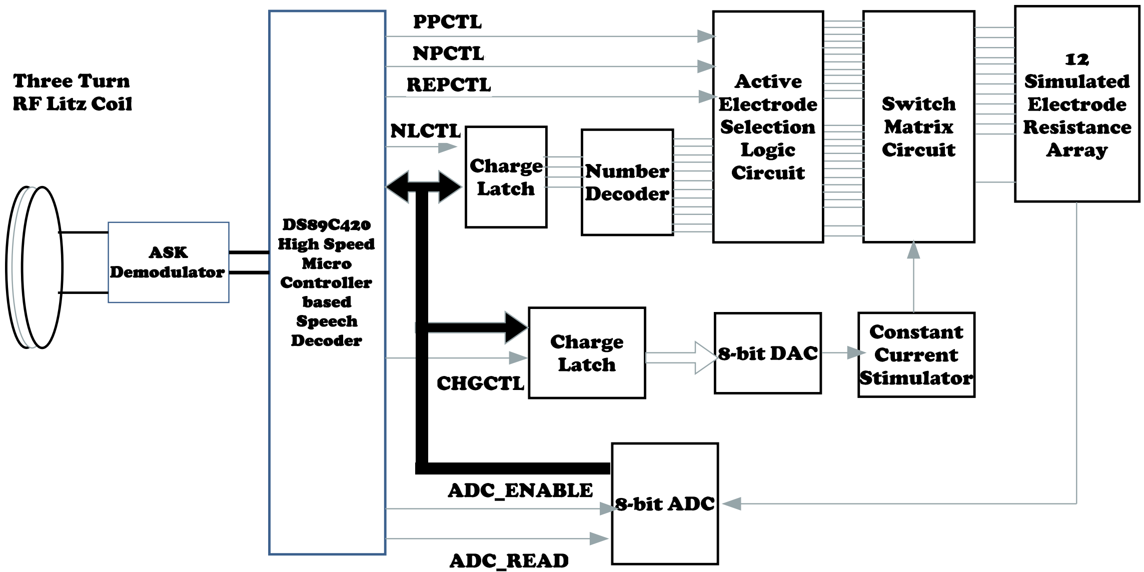

Figure-1: Block diagram of the Receiver Stimulator for Auditory Prosthesis.

Decoder will perform any one of these two functions. Speech decoder receives the data bytes as per the protocol adapted for BWSP. The I/O pins of DS89C420 are configured as follows: one port for bi-directional port, one output port for required control signals.

The port P1 of DS89C420 is connected to two 8-bit edge-triggered D-type flip-flops as buffers with the output-control (OC) input. These two buffers are controlled by the two control signals: Number Latch Control (NLCTL) and Charge Control (CHGCTL) which are generated by the DS89C420 microcontroller for enabling or transferring the information to the respective buffer whenever it is needed.

Only 4-bit output of number latch is connected to 4-to-16 line decoder with latched inputs. Only 12 out of 16 output lines are used for selection of electrode lines. The 12 line outputs of the Number decoder are connected to the Active Electrode Selection Logic Circuit, which is a combinational logic circuit used to generate two pairs of control signals for 12 switches, one pair for the positive side of the bi-phasic pulse generation and other pair for negative side of the pulse generation. In addition to this, it generates switch control signals for reference electrode.

The 8-bit data stored in the charge buffer specifies amount of stimulus current amplitude to be stimulated. The output of the charge buffer is connected to 8-bit Digital to Analog Converter DAC0800. The DAC converts the 8-bit digital value into corresponding analog voltage as output. The

2. Hardware Description

The Laboratory model for RSAP that consists of RF ASK receiver, Stimulus Generator, active electrode decoder, Stimulus buffer, 8-bit Digital to Analog Converter, constant current generator, active electrode selection logic driver, switch matrix and 12 simulated electrode resistance arrays is shown in figure-1.

The ASK Demodulator receives the high-speed serial data at around 172 Kbps rate from the 2 turn secondary Platinum iridium (Pt-Ir) coil and reconstructs corresponding digital signal of encoded speech data and fed to the serial receive input of Speech Decoder. Demodulation of ASK signal is a three stage process which consists of envelope detector, threshold detector and load driver. Envelope detector is simple diode detector which extracts low-high signal variations of 4MHz Carrier wave with a dc offset. The threshold detector is Schmitt trigger circuit which detects whether it is logic '0' or logic '1'. Final stage of Load driver is a buffer consists of two cascaded inverters to get noise free digital TTL signal.

Speech Data Decoder based on Dallas Semiconductor's 8-bit ultra-high-speed flash microcontroller DS89C420 that executes one instruction per clock cycle with 33MHz clock, meeting the demand of real time processing of the speech signals. The High-speed and High performance output of the DAC is connected to the Constant Current Stimulator which gives the constant current according to the input voltage. It maintains the constant current for load resistance up to 10K ohms. Constant current generator generates the current for 0 to 1mA for the input of 8-bit data in the charge buffer ranging from 00 to FF hexadecimal value. This constant current is given as stimulus to the switch matrix driver. Now the current flows across the electrode contact with reference to the reference electrode based on the selected electrode. By properly sending the required control signals to the switches foe closing, the constant current flows across the selected electrode contacts with respect to the reference electrode.

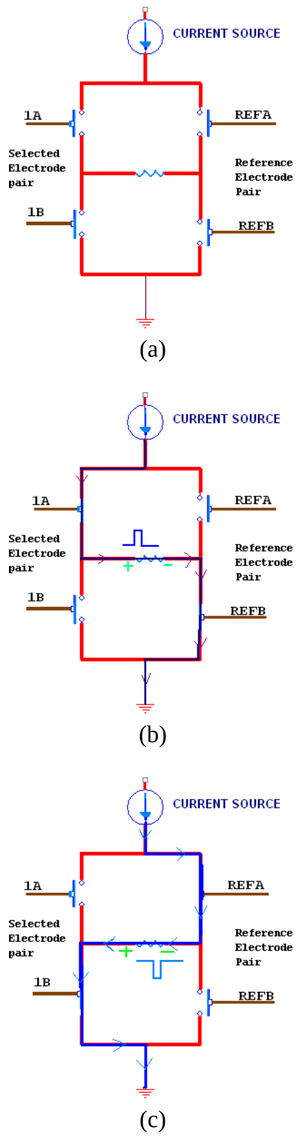

Fig.2 (a) Generation of biphasic pulses using H-matrix architecture. (b) Positive amplitude generation and (c) negative amplitude generation.

The one stage of electrode switching matrix arrangement is as shown in figure-2a based on H-architecture [12]. The H-architecture switches between two opposite pairs of analog switches delivering stimulation current in one direction by closing a pair of switches of the selected electrode from one group (e.g. 1A) and the reference electrode (REFB) and other direction delivering another pair of the selected electrode from second group (e.g. 1B) and the reference electrode (REFA). This circuit switching allows the delivery of the stimulus charge based on the current flow through the simulated electrode resistances. Figure -2b shows the generation of positive amplitude of bi-phsasic pulse as the current flows from the path 1A – resistor-REFB path and Figure-2C shows the negative amplitude of bi-phasic pulse as the current passes though the path REFA-resistor-1B.

3. Software Description

The software design is based on top-down approach that identifies the major components of the system, decomposing them into their lower-level components and iterating until the desired level of details is achieved. The two important functional modules such as Speech Processing module and Impedance Telemetry module are described by using the flowchart as shown in figure-3.

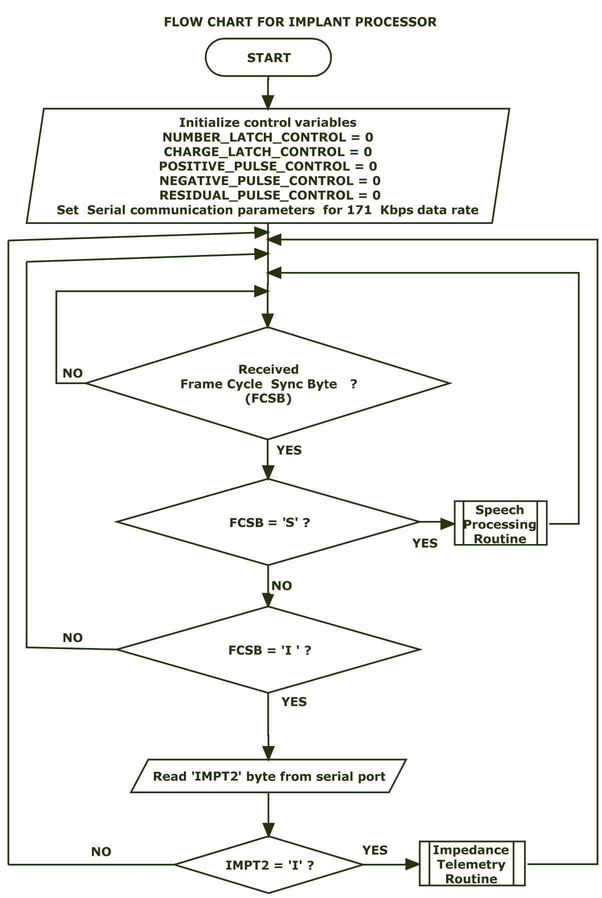

Figure-3: Flowchart for the overall function of RSAP

The main function of Speech Processing module is to receive stimulus information of one electrode at a time that contains electrode number and electrode charge and stimulate the corresponding electrode with given charge in the stimulus information. The function of Impedance Telemetry module function is to read the impedance of the electrodes and send this information to Impedance Telemetry module. This paper covers the speech data processing function of speech data decoding and stimulation.

The embedded software program in the DS89C420 microcontroller performs the tasks such as Speech decoder and Impedance telemetry processing. The NLCTL and CHGCTL are initialized to Logic '1', Pulse control signals are initialized to logic '0' and the parameters for the serial port of the microcontroller are initialized to 172Kbps baud rate. The reconstructed serial data from the ASK demodulator is received by the receive pin (rx) of DS89C420. The data format received from the BWSP is shown figure-4.

FCSB	EL1	CH1	EL2	CH2	**….**	EL8	CH8

Figure-4: Protocol format sent by the BWSP

The data format contains Frame Cycle Sync Byte (FCSB), active eight pairs of electrode numbers (EL_i) and electrode charge (CH_i) for 8 electrodes. The BWSP sends the speech data in data format in figure-4 continuously. The RSAP takes two bytes of information that contains the electrode number and the charge. It places the first byte first on the port and issues the NLCTL signal enabling the buffer to load the new value which is used as input to the electrode selection circuit and places the next byte into the port that contains the charge to be stimulated and issues a pulse to the CHGCTL signal which loads the new values served as input to the DAC and current stimulator. By setting the timer values of 14us for both positive and negative pulses of biphasic pulse with associated control signals, biphasic pulses are generated .The operation of overall system is represented by a flowchart as shown in figure-5.

3.1. Impedance Telemetry functions:

The impedance telemetry function is explained with the help of flowchart as shown in Figure-6. If the received FCSB is 'I' it indicates that the function is impedance telemetry function. It reads the impedance of each channel by stimulating each channel with "0xFF", using ADC and store each resistance/impedance value in the internal memory. After reading resistance (RES_i) of each channel, it prepares the response byte as shown in figure-7.

RES	EL1	RES1	**….**	EL8	RES8

Figure-7: Response format sent by the IRS

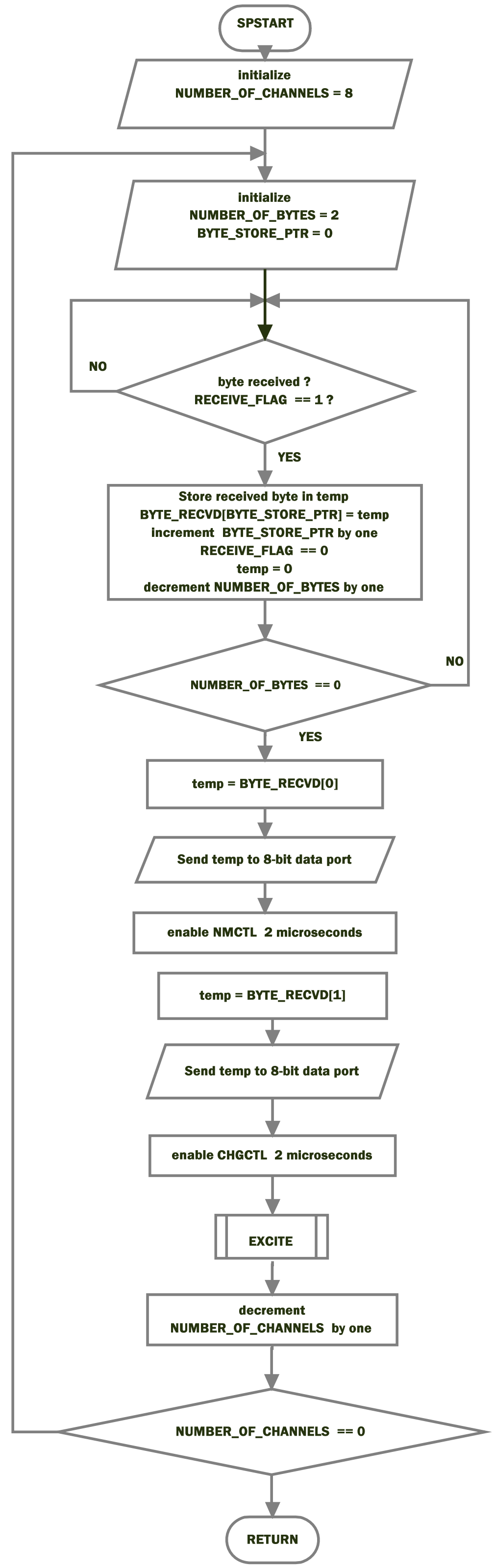

Figure-5: Flowchart for the Speech Processing routine

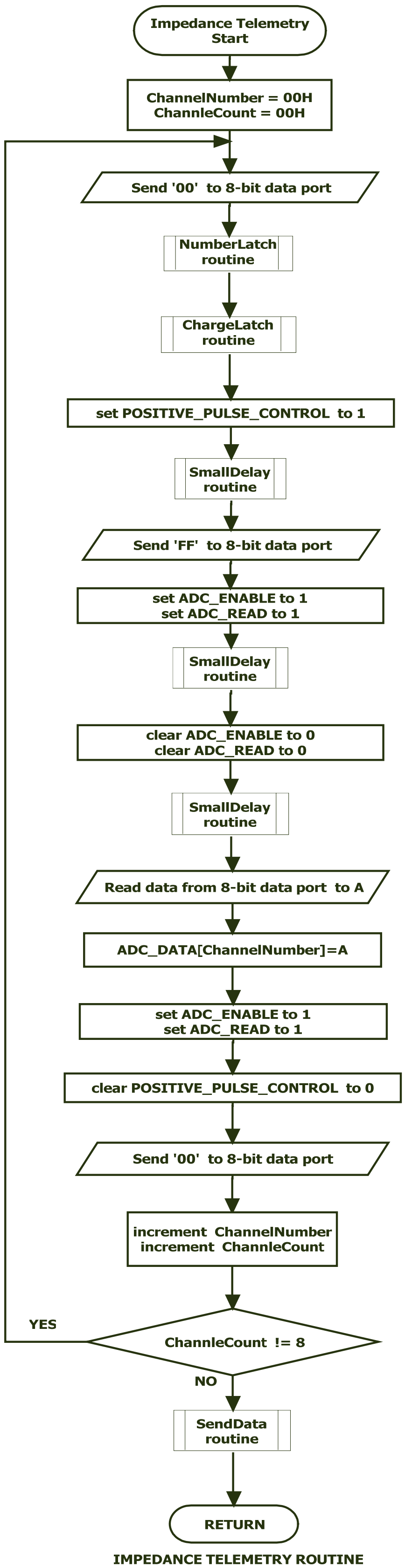

Figure-6: Flowchart for impedance telemetry routine

4. Results

The functionality of the prototype model is tested and validated using test data samples and real-time speech samples. Test samples for speech processing routine are generated by using laboratory model of BWSP. The BWSP is initially programmed for 8 channel Speech processor and observed satisfactory performance. The several identified test data patterns are applied to the RSAP and observed the respective electrode stimulation signals at simulated electrode resistance array. One of the sample test pattern is by sending equal charge to all the electrodes. The corresponding stimulation outputs across the electrodes with different load resistance values are shown in figure-8.

Impedance telemetry (IMT) function is tested by using laboratory model of IMT module after issuing the impedance telemetry command to RSAP and read the resistance values sent by the RSAP as per the response format, stored in the internal memory of IMT. By using UP/DOWN key of the IMT module, the resistance values of all 12 electrodes are observed. The process is repeated several times by varying the simulated resistances of electrodes and observed the resistance values as expected. This RSAP is also tested with the CPS software and IMT module. By using the CPS software, the resistance values of each patient are read and stored in the database for future use. CPS software is also used to generate the stimulus pulses of varying amplitudes to determine the patient threshold and most comfort values.

5. conclusions

The Microcontroller Based Prototype model of RSAP for Hearing Impaired research has been developed. The system has been tested by using simulated test data. The Laboratory model of Body Speech Processor is used to test 8-channel auditory prosthesis by sending the encoded ASK modulated serial data bits to RSAP for real-time speech signal. The RSAP is validated by stimulating the selected electrodes as the simulated electrode resistance array and observed satisfactory results. The impedance telemetry feature is also tested using the Laboratory model of IMT module. Individual channels are stimulated with associated charge to determine the patient thresholds. The conversion from prototype model to CMOS ASIC model is under progress.

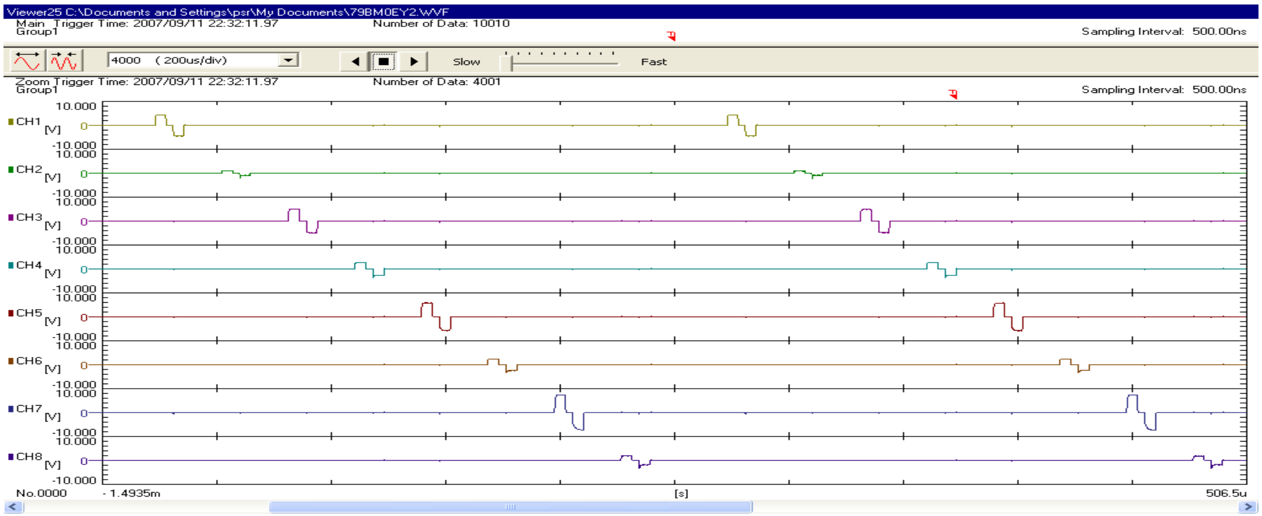

Figure-8: Responses of the 8 electrodes across the simulated electrode resistance array

Acknowledgments

The authors wish to thank Dr. V. Bhujanga Rao, Director, NSTL, Visakhapatnam who provided suitable hardware and software tools for successful completion of laboratory prototype of Receiver Stimulator for Auditory Prosthesis. This work is supported by defense R & D organization – NSTL-Visakhapatnam, INDIA under the contract no. NSTL/WI/CI dated 26 February 2009.

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